International Journal of Innovative Computing, Information and Control
Volume **1**, Number **2**, June **2005**

 ISSN 1349-4198
pp. **193–202**

AN APPLICATION OF FUZZY INFERENCE CIRCUIT FOR ANALOG PHASE LOCKED LOOP

Kuniaki Fujimoto and Hirofumi Sasaki

Department of Electrical and Electronics System
School of Engineering, Kyushu Tokai University
9-1-1, Kumamoto 862-8652, Japan
{ kfuji, hsasaki }@ktmail.ktokai-u.ac.jp

Received October 2004; revised February 2005

Abstract. *There is a technical and economical problem to be solved when the large value resistors and capacitors are realized in the integrated circuit. In this paper, we propose a fuzzy phase locked loop (PLL) in which a fuzzy inference circuit is used instead of a loop filter composed of resistors and capacitors in an analog PLL. This circuit can be integrated into a small size chip even in the low frequency domain and the characteristics of pull-in, jitter and synchronous range for the proposed circuit are similar to those of the conventional analog PLLs.*
Keywords: Phase locked loop, Fuzzy reasoning, Field programmable gate array, Integrated circuit

1. **Introduction.** A phase locked loop (PLL) is fundamentally composed of a phase comparator (PC), a loop filter (LF) and a voltage controlled oscillator (VCO). The PLL is a feedback circuit that controls the VCO by detecting the phase difference between input and output signals and by assigning the difference value of zero. PLL is one of the essential functional circuits for synchronizing signals, automatic frequency control, frequency conversion and synthesis, narrow bandwidth reception and signal tracking, which are commonly used as parts of TV sets, audio equipment, peripheral equipment for personal computers, communication equipment, measuring instruments, and other devices. The vital characteristics of PLLs are quick pull-in, low jitter and a broad range of synchronization. Many reports have been published about how these characteristics can be improved [1-8].

On the other hand, with respect to PLLs intended for use at low frequencies, it is necessary to use large value resistors and capacitors in the loop filter to obtain the DC voltage needed for controlling the VCO. There is a technical and economical problem to be solved when the large value resistors and capacitors are realized in the integrated circuit.

In this paper, we demonstrate that these problems can be solved by substituting the loop filter section of the conventional analog PLL with a fuzzy inference circuit [9-11]. The circuit is designed with a hardware description language, Verilog-HDL. Thus, it can be more easily incorporated into integrated circuits. Furthermore, the circuit scale is made smaller by designing the circuit with the membership function circuits and the arithmetic circuits based on fixed point binary insides the fuzzy inference circuit. The characteristics