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FAST DEBLOCKING FILTER IMPLEMENTATION METHOD FOR H.264/AVC

Tian Song, Yoshinori Hayashi and Takashi Shimamoto

Department of Institute of Technology and Science
Graduate School of Engineering
Tokushima University
Minami-Jyosanjima 2-1, Tokushima City, 770-8506, Japan
{ tiansong; hayasi1219; simamoto }@ee.tokushima-u.ac.jp

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Abstract. *In this work, a fast implementation method for deblocking filter of H.264/AVC and its architecture are proposed. The proposed method makes use of the correlation of the adjacent pixels to decrease the redundant processing cycles. Simulation results show that using proposed method, the average coding cycles for one macroblock is reduced to 170. It is fast than that of the previous works which considered that the least number of filtering cycles for one macroblock are 192. This work also provides an efficient architecture for the proposed method in which a parallel memory access solution and a novel comparison module are proposed. The power consumption is also considered in our design of filtering core architecture. Implementation results show that the proposed architecture can be realized by about 30K gates.*
Keywords: H.264/AVC, Deblocking filter, Architecture

1. **Introduction.** Compared with previous video coding standards such as MPEG-2 and MPEG-4, H.264/AVC [1][2] succeeded to achieve higher compression efficiency by introducing some new coding tools. The coding efficiency of H.264/AVC is widely acknowledged by scientific and industrial fields. However, because H.264/AVC inherits a macroblock based MC-DCT structure it inevitability induces block artifact by the discrete quantization approach. The block artifact may occur at the edge of macroblocks and significantly impact picture quality. Numbers of filter algorithms have been proposed to improve the subjective video quality[3][4]. H.264/AVC introduced a hardware-friendly filter, namely deblocking filter, to eliminate this block artifact. Figure 1 shows a typical processing flow of the H.264/AVC encoder and Figure 2 shows a typical H.264/AVC decoder.

In these two figures, Q and IQ represent quantization and inverse quantization modules. DCT and IDCT indicate discrete cosine transform and inverse discrete cosine transform modules. VLC and VLD are variable length coding and variable length decoding modules. The motion compensation including the motion estimation is performed in the MC and ME modules respectively. DF module is in charge of a filtering operation between sub-blocks. It has to be implemented in both encoder and decoder side. However, this deblocking filtering is a complexity intensive process because the filtering process is performed at the edge of all adjacent macroblocks and sub-macroblocks.

Some previous works have provided several fast filtering solutions for the implementation of deblocking filter. Huang's proposal [5] provides three optional architectures from the viewpoint of the memory access efficiency. In this work single-port and dual-port memory access solutions are discussed and the coding ability of 614 cycles/macroblock is achieved. Some other discussions have been made generally concerning the filtering order, memory size and registers [6]-[9]. In Liu's method [6], the filtering order is optimized and