A FIBONACCI-TYPE DC-AC INVERTER DESIGNED BY SWITCHED CAPACITOR TECHNIQUE

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ABSTRACT. To use electric appliances inside vehicles, a Fibonacci switched-capacitor (SC) DC-AC inverter is proposed in this paper. Various SC DC-AC inverters were proposed as previous studies. Unlike common DC-AC inverters containing inductors or transformers, the SC inverters require no magnetic components. Among others, an SC DC-AC inverter based on a series-parallel type converter is famous as a conventional DC-AC inverter. However, the conventional DC-AC inverters require many capacitors to generate a staircase AC waveform. To reduce the number of capacitors, the proposed inverter is controlled so that the voltage ratio of capacitors becomes the ratio of a Fibonacci number. The proposed inverter generates the staircase AC waveform by combining some of these capacitors in series. Therefore, unlike the conventional SC DC-AC inverter based on a series-parallel type converter, the proposed inverter can provide the staircase AC waveform by a smaller number of capacitors. In this paper, the validity of the proposed inverter is verified by the theoretical analysis. The simulated results show the property and the effectiveness of the proposed inverter. The feasibility of the proposed inverter is demonstrated in circuit experiments.

Keywords: DC-AC inverter, Switched capacitor circuits, Inductor-less circuits, Fibonacci number

1. Introduction. In recent years, marketed DC-AC inverters are used for using electric appliances in vehicle. The DC-AC inverter can generate AC waveform from the input low DC voltage of a cigarette socket. However, the marketed DC-AC inverters have a problem that the output waveform of the marketed DC-AC inverters is a square waveform which is far from a sinusoidal waveform. To generate a sinusoidal waveform as an output voltage, Sanchis et al. proposed a Buck-boost DC-AC inverter [1] and its control method. The Buck-boost DC-AC inverter has two Buck-boost DC-DC converter blocks, and it can offer smooth sinusoidal waveform with high power efficiency. However, the voltage stress of the entire system is high due to an off-set voltage which is higher than its input voltage. To solve this problem, Kim et al. proposed an embedded Z-source DC-AC converter [2-4] and its control method. By using the embedded Z-source DC-AC converter, the voltage stress can be reduced owing to the control method of the embedded Z-source DC-AC converter. However, these conventional DC-AC inverters are heavy and bulky, because the DC-AC inverters have magnetic components. To solve these problems, a switched-capacitor (SC) DC-AC inverter has been proposed by many researchers. Unlike the common DC-AC
inverter containing magnetic components, the SC DC-AC inverter can generate an AC voltage without the use of magnetic components. The SC DC-AC inverter can offer not only small circuit size but also small effects of the electromagnetic inference (EMI).

For this reason, Ueno et al. suggested the voltage equation type SC DC-AC inverter [5]. Following this, Oota et al. proposed a bidirectional SC DC-AC inverter [6]. By using a series-parallel type inverter [7], these inverters can generate a staircase AC waveform. However, many circuit components are required in order to provide big number of steps of the staircase waveform. That is because the steps of the staircase waveform are proportional to the number of capacitors. To improve this drawback, Eguchi et al. suggested the DC-AC converter using ring-type converter [8,9]. The ring-type converter can provide flexible output voltages by changing connection-types of series capacitors. However, the ring-type converter cannot realize high voltage ratio without many capacitors. To reduce the number of capacitors, Chang proposed the multistage switched-capacitor-voltage-multiplier (SCVM) DC-AC inverter [10]. The SCVM inverter can generate a staircase AC waveform by the small number of capacitors due to series-connected SC cells. However, all capacitor voltages of these conventional DC-AC inverters are the same.

In this paper, in order to provide a staircase AC waveform formed by many steps, a Fibonacci SC DC-AC inverter is proposed. Unlike the conventional SC DC-AC inverters, the voltage ratio of capacitors is the ratio of the Fibonacci number. By combining some of these capacitors in series, the proposed inverter generates the staircase AC waveform by a small number of capacitors, because the voltage of the charged capacitors of the proposed inverter is higher than that of the conventional SC DC-AC inverter. To confirm the validity of the proposed SC DC-AC inverter, theoretical analysis, simulation and experiments are performed.

The rest of this paper is organized as follows. In Section 2, the circuit configurations of the conventional inverter and the proposed inverter are presented. In Section 3, the validity of the proposed inverter is clarified by the theoretical analysis. To verify the property and the effectiveness of the proposed inverter, the simulated results are shown in Section 4. In Section 5, the feasibility of the proposed inverter is demonstrated by the experimental results. Finally, conclusion and future study are drawn in Section 6.

2. Circuit Configuration.

2.1. Conventional inverter. Figure 1 shows the conventional SC DC-AC inverter [6]. The conventional inverter is based on the series-parallel type converter. As Figure 1 shows, the conventional inverter has no magnetic components. In the conventional inverter, all the capacitor voltages are $V_{in}$. To generate a staircase AC waveform, the bi-direction switches are controlled like a step-up DC-DC converter. Therefore, the output voltage $V_o$ of each step is expressed by conventional inverter having no magnetic components. In the conventional inverter, all the capacitor voltages are $V_{in}$. To generate a staircase AC waveform, the bi-direction switches are controlled like a step-up DC-DC converter. Therefore, the output voltage $V_o$ of each step is expressed by

$$V_o = mV_{in}, \quad \text{where} \quad m = \{1, 2, \ldots, N + 1\}. \quad (1)$$

In (1), $N$ is the number of main capacitors. Concretely, the conventional inverter generates the staircase waveform formed by 8 (= $(3 + 1) \times 2$) steps in the case of 3 stages. The staircase waveform $V_{out}$ is obtained through the full bridge circuit. Table 1 shows the operations of the conventional inverter during one cycle. In the case of state-$T_1$, bi-directional switches $\varepsilon$ are turned on. Then, each capacitor of the sub circuit-1 is charged, and the sub circuit-2 generates stepped-up voltage. Therefore, as Table 1 shows, the state of the sub circuit-1 is a charging process and the state of the sub circuit-2 is
2. Proposed inverter. Figure 2 shows the proposed Fibonacci SC DC-AC inverter. Unlike the conventional SC DC-AC inverter, the voltage ratio of capacitors is the ratio of a Fibonacci number. Concretely, the voltage of the $i$-th ($i = 1, 2, 3$) capacitor is $i \times V_{in}$ in the case of 3 stages. In the proposed inverter, the output voltage $V_o$ of each step is expressed as

$$V_o = nV_{in}, \quad \text{where} \quad n = \{1, 2, \ldots, 7\}. \quad (2)$$

As (2) shows, the proposed inverter can generate the staircase waveform formed by 14 ($= 7 \times 2$) steps in the case of 3 stages owing to high voltage ratio of each capacitor. Therefore, the proposed inverter can offer the staircase AC waveform by a smaller number of capacitors. Table 2 shows the timing of the operation process. As Table 2 shows, the proposed inverter has three processes: 1) charging process; 2) transferring process; and 3) averaging process. By repeating these three processes mutually, the voltage ratio of each capacitors becomes the ratio of a Fibonacci number. In addition, as Table 2 shows, by shifting the timing of each process of the inverter block-2 against that of the inverter.
Figure 2. Proposed SC DC-AC inverter

Table 2. Operations of the proposed inverter in the case of the 7x step-up

<table>
<thead>
<tr>
<th>State</th>
<th>Inverter block-1</th>
<th>Inverter block-2</th>
<th>On</th>
<th>Off</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_1$</td>
<td>Charging process</td>
<td>Transferring process</td>
<td>$S_{11}^{1}, S_{21}^{1}, S_{31}^{1}, S_{41}^{1}, S_{12}^{1}, S_{22}^{1}, S_{32}^{1}, S_{42}^{1}$</td>
<td>Others</td>
</tr>
<tr>
<td>$T_2$</td>
<td>Transferring process</td>
<td>Charging process</td>
<td>$S_{11}^{1}, S_{21}^{1}, S_{31}^{1}, S_{41}^{1}, S_{12}^{1}, S_{22}^{1}, S_{32}^{1}, S_{42}^{1}$</td>
<td>Others</td>
</tr>
<tr>
<td>$T_3$</td>
<td>Averaging process</td>
<td>Transferring process</td>
<td>$S_{11}^{1}, S_{21}^{1}, S_{31}^{1}, S_{41}^{1}, S_{12}^{1}, S_{22}^{1}, S_{32}^{1}, S_{42}^{1}$</td>
<td>Others</td>
</tr>
<tr>
<td>$T_4$</td>
<td>Transferring process</td>
<td>Averaging process</td>
<td>$S_{11}^{1}, S_{21}^{1}, S_{31}^{1}, S_{41}^{1}, S_{12}^{1}, S_{22}^{1}, S_{32}^{1}, S_{42}^{1}$</td>
<td>Others</td>
</tr>
</tbody>
</table>

block-1, the transferring processes of the inverter block-1 appear in state-$T_2$ and $T_4$. On the other hand, the inverter block-2 becomes the transferring process during state-$T_1$ and $T_3$. Therefore, there are the transferring processes at all states.

Figure 3 shows the current flow of the proposed inverter in each state. In the proposed inverter, $C_1^1$ and $C_1^2$ are charged with the input voltage, $C_2^1$ and $C_2^2$ are charged with 2 times the input voltage (the input voltage plus the voltage of first capacitor $C_1^1$ or $C_2^1$), $C_1^3$ and $C_2^3$ are charged with 3 times the input voltage (the input voltage plus the voltage of the second capacitor $C_2^1$ or $C_2^2$). The voltage of each capacitor is charged by repeating the states shown in Figure 3. In Figure 3(a), capacitor $C_1^1$ and $C_1^2$ are charged. Each capacitor is charged with the following method: $C_1^1$ is charged with the input voltage and $C_1^3$ is charged with 3 times the input voltage. On the other hand, the inverter block-2 generates 7x stepped-up input voltage by connecting all the capacitors in series. In Figure 3(b), the inverter block-1 generates 7x times stepped-up input voltage. On the other hand, the state of the inverter block-2 shown in Figure 3(b) becomes the same state as that of the inverter block-1 in Figure 3(a). In Figure 3(c), capacitor $C_2^1$ is charged with 2 times the input voltage, which is the input voltage plus the voltage of $C_1^1$. At that time, the inverter block-2 becomes the transferring process. Finally, in Figure 3(d), capacitor $C_2^2$ is
The proposed inverter is much smaller than that of conventional inverter owing to the voltage ratio of the proposed inverter. From these results, the proposed inverter can reduce 40% of the circuit components between the conventional inverter and the proposed inverter in the case of 7x step-up. As Table 3 shows, the conventional inverter requires 78 circuit components, because the conventional inverter must be expanded to 7 stages to generate the 7 stepped-up voltage. On the other hand, the proposed inverter requires 38 circuit components to offer 7x stepped-up voltage. Therefore, the number of the circuit components of the proposed inverter is much smaller than that of conventional inverter owing to the voltage ratio of the proposed inverter. From these results, the proposed inverter can reduce 40% of the circuit components between the conventional inverter and the proposed inverter in the case of 7x step-up.

In the proposed inverter, two capacitors and eight bi-directional switches are required to charged in the same way as the $C_2$ of Figure 3(c). Therefore, the voltage of $C_2$ is 2 times the input voltage. Then, the inverter block-1 is transferring process in this state. By repeating these four processes, the proposed inverter offers the stepped-up voltage in all states. In this discussion, the operation of the proposed inverter in the case of 7x step-up was explained. Of course, the $n$ ($n = \{1, 2, \ldots, 7\} \times$ stepped-up voltage is obtained by combing some of main capacitors in series.

In the proposed inverter, two capacitors and eight bi-directional switches are required to build one stage of the proposed inverter. Table 3 shows the comparison of the number of circuit components between the conventional inverter and the proposed inverter in the case of 7x step-up. As Table 3 shows, the conventional inverter requires 78 circuit components, because the conventional inverter must be expanded to 7 stages to generate the 7 stepped-up voltage. On the other hand, the proposed inverter requires 38 circuit components to offer 7x stepped-up voltage. Therefore, the number of the circuit components of the proposed inverter is much smaller than that of conventional inverter owing to the voltage ratio of the proposed inverter. From these results, the proposed inverter can reduce 40% of the circuit components between the conventional inverter and the proposed inverter in the case of 7x step-up. In the proposed inverter, two capacitors and eight bi-directional switches are required to charged in the same way as the $C_2$ of Figure 3(c). Therefore, the voltage of $C_2$ is 2 times the input voltage. Then, the inverter block-1 is transferring process in this state. By repeating these four processes, the proposed inverter offers the stepped-up voltage in all states. In this discussion, the operation of the proposed inverter in the case of 7x step-up was explained. Of course, the $n$ ($n = \{1, 2, \ldots, 7\} \times$ stepped-up voltage is obtained by combing some of main capacitors in series.

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Table 3. Comparison of the number of circuit components

<table>
<thead>
<tr>
<th>The number of components</th>
<th>Conventional inverter (7 stages)</th>
<th>Proposed inverter (3 stages)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage gain</td>
<td>7x step-up</td>
<td></td>
</tr>
<tr>
<td>Capacitor</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>Switch</td>
<td>62</td>
<td>30</td>
</tr>
<tr>
<td>Total</td>
<td>78</td>
<td>38</td>
</tr>
</tbody>
</table>

(= 78 – 38) circuit components in the case of 7x step-up. Furthermore, according to the increase of the number of circuit stages, this difference increases. Therefore, the proposed inverter can achieve smaller size than the conventional inverter owing to small circuit components.

3. Theoretical Analysis. To clarify the validity of the proposed inverter, theoretical analysis is performed, where the equivalent circuit is assumed as a four-terminal equivalent model reported in [11]. In the case of the 7x step-up conversion, the theoretical analysis is discussed. In the theoretical analysis, the following things are assumed: (1) bi-directional switch is defined by an ideal switch, which has an on-resistance \( R_{on} \); and (2) time constant is much larger than the period of clock pulses.

Firstly, the behavior of the inverter block-1 is discussed. In steady state, the differential value of the electric charge in \( C_{kj} \) \((k = 1, 2, 3, 0)\) is expressed to

\[
\sum_{i=1}^{4} \Delta q_{T_i}^k = 0, \quad \text{where} \quad T = \sum_{i=1}^{4} T_i = 4T_s \\
\quad \text{and} \quad T_1 = T_2 = T_3 = T_4 = T_s. \tag{3}
\]

In (3), \( \Delta q_{T_i}^k \) denotes the electric charge of the \( k \)-th capacitor in State-\( T_i \) and \( T_s \) is the interval of each state. In the steady state of the inverter block-1, the differential values of electric charge in \( V_i \) and \( V_o \), \( \Delta q_{T_i,V_i} \) and \( \Delta q_{T_i,V_o} \), satisfy as follows:

State-\( T_1 \): \( \Delta q_{T_1,V_i} = \Delta q_{T_1}^1 - \Delta q_{T_1}^2, \quad \Delta q_{T_1,V_o} = \Delta q_{T_1}^0, \quad \text{and} \quad \Delta q_{T_1}^2 = -\Delta q_{T_1}^3, \tag{4} \)

State-\( T_2 \): \( \Delta q_{T_2,V_i} = -\Delta q_{T_2}^1, \quad \Delta q_{T_2,V_o} = \Delta q_{T_2}^3 + \Delta q_{T_2}^0, \quad \text{and} \quad \Delta q_{T_2}^1 = \Delta q_{T_2}^2. \tag{5} \)

State-\( T_3 \): \( \Delta q_{T_3,V_i} = -\Delta q_{T_3}^1, \quad \Delta q_{T_3,V_o} = \Delta q_{T_3}^0, \quad \Delta q_{T_3}^1 = -\Delta q_{T_3}^2, \quad \text{and} \quad \Delta q_{T_3}^3 = 0. \tag{6} \)

State-\( T_4 \): \( \Delta q_{T_4,V_i} = -\Delta q_{T_4}^1, \quad \Delta q_{T_4,V_o} = \Delta q_{T_4}^3 + \Delta q_{T_4}^0, \quad \text{and} \quad \Delta q_{T_4}^1 = \Delta q_{T_4}^2. \tag{7} \)

From (3)-(7), the average input current and the average output current can be obtained as

\[
\bar{I}_i = \frac{1}{T} \left( \sum_{i=1}^{4} \Delta q_{T_i,V_i} \right) = \frac{\Delta q_{V_i}}{T} \quad \text{and} \quad \bar{I}_o = \frac{1}{T} \left( \sum_{i=1}^{4} \Delta q_{T_i,V_o} \right) = \frac{\Delta q_{V_o}}{T} \tag{8}
\]

where \( \Delta q_{V_i} \) and \( \Delta q_{V_o} \) are electric charges in the input and output, respectively. Substituting (3)-(7) into (8), the relation between the input current and output current is
expressed to the following equation:

\[ T_i = -7T_o, \quad \text{where} \quad \Delta qV_i = -14\Delta q^3T_2 \]

and \( \Delta qV_o = 2\Delta q^3T_2. \) \( (9) \)

Next, the consumed energy in one period is considered. Using (3)-(7), the consumed energy of the inverter block can be expressed as

\[ W_T = \sum_{i=1}^{4} W_{T_i} = \frac{168R_{on}}{T} (\Delta qV_o)^2, \]

\( (10) \)

where \( W_{T_i} = \frac{R_{on}}{T_s} (\Delta q^1T_i - \Delta q^2T_i)^2 + \frac{R_{on}}{T_s} (\Delta q^2T_i)^2 + \frac{3R_{on}}{T_s} (\Delta q^2T_1)^2, \)

\( W_{T_2} = \frac{4R_{on}}{T_s} (\Delta q^2T_2)^2, \)

\( W_{T_3} = \frac{2R_{on}}{T_s} (\Delta q^2T_3)^2 + \frac{R_{on}}{T_s} (\Delta q^2T_3)^2, \)

and \( W_{T_4} = \frac{4R_{on}}{T_s} (\Delta q^2T_4)^2. \)

Here, it is known that the general equivalent circuit of the capacitor-based voltage converter can be expressed by the Kettenmatrix [10]. In the general equivalent circuit, \( W_T \) can be defined as

\[ W_T := \left( \frac{\Delta qV_o}{T} \right)^2 \cdot R_{SC} \cdot T, \]

\( (11) \)

where \( R_{SC} \) is called the SC resistance. By combining (9)-(11), the equivalent circuit for the 7x step-up mode is expressed as follows:

Inverter block:

\[ \begin{bmatrix} V_i \\ T_i \end{bmatrix} = \begin{bmatrix} 1/7 & 0 \\ 0 & 7 \end{bmatrix} \begin{bmatrix} 1 & R_{SC} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_o \\ -I_o \end{bmatrix} \]

\( (12) \)

Proposed inverter:

\[ \begin{bmatrix} V_{in} \\ T_{in} \end{bmatrix} = \begin{bmatrix} 1/7 & 0 \\ 0 & 7 \end{bmatrix} \begin{bmatrix} 1 & R_{SC}/2 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_{out} \\ -I_{out} \end{bmatrix} \]

\( (13) \)

where \( R_{SC} = 168R_{on}. \)

Therefore, the efficiency \( \eta \) and output voltage \( V_{out} \) of the proposed inverter can be obtained as

\[ \eta = \frac{(T_{out})^2 R_L}{(I_{out})^2 R_L + (I_{out})^2 R_{SC}/2} = \frac{R_L}{R_L + R_{SC}/2} \]

and

\[ V_{out} = \frac{R_L}{R_L + R_{SC}/2} \times 7V_{in}. \]

\( (14) \)

The list of theoretical results is shown as Table 4. From these results, the validity of the proposed inverter was clarified by the theoretical analysis.

<table>
<thead>
<tr>
<th>Gain</th>
<th>( R_{SC} )</th>
<th>Gain</th>
<th>( R_{SC} )</th>
<th>Gain</th>
<th>( R_{SC} )</th>
<th>Gain</th>
<th>( R_{SC} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1x</td>
<td>2 ( R_{on} )</td>
<td>2x</td>
<td>12 ( R_{on} )</td>
<td>3x</td>
<td>26 ( R_{on} )</td>
<td>4x</td>
<td>50 ( R_{on} )</td>
</tr>
<tr>
<td>5x</td>
<td>118 ( R_{on} )</td>
<td>6x</td>
<td>120 ( R_{on} )</td>
<td>7x</td>
<td>168 ( R_{on} )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
4. Simulation. To confirm the characteristic of the proposed inverter, the simulation is performed by the simulation program with integrated circuit emphasis (SPICE) simulations. Figure 4 shows the simulated results of the inverter block in the proposed inverter. In Figure 4, the SPICE simulations were performed under conditions that $V_{in} = 20V$, $C_{kj} = 150\mu F$ ($k = 1, 2, 3, 6$) and $R_{on} = 0.1\Omega$, $T = 20\mu s$, and $T_s = 5\mu s$. As Figure 4 shows, the theoretical results are corresponding to the SPICE simulated results. Therefore, the theoretical formulas obtained by the theoretical analysis will be helpful to estimate the characteristics of the proposed inverter.

Figure 5 shows the simulated results of the proposed inverter. Figure 5(a) shows the simulated staircase AC waveform when $R_L$ is 1kΩ. To generate the staircase 100V@50Hz

![Figure 4](image1.png)

**Figure 4.** Simulated results of the inverter block: (a) output voltage and (b) power efficiency

![Figure 5](image2.png)

**Figure 5.** Simulated results of the proposed inverter: (a) output waveform and (b) power efficiency
waveform, the parameters were set to $V_{in} = 20V$, $C_{kj} = 10\mu F$, $R_{on} = 0.1\Omega$, $T = 20\mu s$, and $T_s = 5\mu s$. The simulated power efficiency as a function of the output power is shown in Figure 5(b). In the range from 2 to 100W, the proposed inverter can offer more than 80% efficiency. As Figure 5(b) also shows, the power efficiency of the conventional inverter is higher than that of the proposed inverter in the range which is more than 10W. On the other hand, the power efficiency of the proposed inverter is higher than that of the proposed inverter in the range which is less than 10W.

5. **Experiments.** To clarify the feasibility of the proposed inverter, experiments are performed. In the experiment, the number of stages of the proposed inverter was set to 3 stages. The experimental conditions of the proposed inverter with 3 stages are as follows: $V_{in} = 12V$ and $T = 2\mu s$. Table 5 shows circuit components of the experimental proposed inverter. As you can see from Table 5, by using an AVR microcontroller ATMEGA 164P, the bi-directional switches are controlled in the experimental inverter. However, the signals, which are generated by the AVR micro controller, cannot control the bi-directional switches due to low output power. Therefore, bootstrap circuits are attached to each switch to drive the bi-directional switches. The bootstrap circuit consists of high-low side driver ICs, diode switches and pumping-up capacitors. In the bootstrap circuit, there is no magnetic component. The bootstrap circuit is controlled by the signal of the AVR micro controller and drives the gate terminal of the bi-directional switches by using a voltage of the pumping-up capacitors. However, there is no charging process for the pumping-up circuit in the operation of the proposed inverter. Therefore, that timing must be added to the operation of the proposed inverter. Figure 6 shows the experimental

<table>
<thead>
<tr>
<th>Parts</th>
<th>Components</th>
<th>Models</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock pulse generator block</td>
<td>Micro controller</td>
<td>AVR ATMEGA 164P</td>
</tr>
<tr>
<td>Bootstrap circuit block</td>
<td>High-low side driver IC</td>
<td>IR2110</td>
</tr>
<tr>
<td></td>
<td>Diode switches</td>
<td>1N4007</td>
</tr>
<tr>
<td></td>
<td>Capacitors</td>
<td>2.2\mu F</td>
</tr>
<tr>
<td>Inverter block</td>
<td>Power switch</td>
<td>TK40E06N1</td>
</tr>
<tr>
<td></td>
<td>Capacitor</td>
<td>100\mu F</td>
</tr>
<tr>
<td>Full-bridge block</td>
<td>Power switch</td>
<td>TK100E10N1</td>
</tr>
<tr>
<td></td>
<td>Load</td>
<td>10kΩ</td>
</tr>
</tbody>
</table>

![Figure 6. One experimental inverter](image-url)
The circuit for charging is designed to charge the pumping-up capacitor of the bootstrap circuit. The circuit is driven when the inverter block is a charging process. The pumping-up capacitors of the bootstrap are charged by turning on the switch $S_d$ during the charging process, because all states of switches $S_{oi}$ ($i = 1, 2, 3, 4$) are off at those timing. Owing to this circuit, the experimental circuit works in practice.

Figure 7 shows the photograph of the experimental inverter. As Table 5 shows, the experimental inverter of Figure 7 was built with commercially available components on a universal board. The size of the universal board is the same as a paper size A5, which is 148mm × 210mm.

Figure 8 shows the measured output waveform of the proposed inverter. As Figure 8 shows, the proposed inverter can generate a staircase AC waveform, where the maximum output voltage is 72.2V and frequency is 57.5Hz. From this result, the experimental inverter can realize the high voltage ratio with the small number of capacitors because
72.2V is about 6 times the input voltage despite the fact that the number of the capacitor is only three. From this result, the feasibility of the proposed inverter has been verified.

6. Conclusions. A Fibonacci switched-capacitor (SC) DC-AC inverter has been proposed in this paper. The characteristics of the proposed inverter were clarified by the comparison with the conventional inverter, the theoretical analysis, the SPICE simulations and the experiments. In the comparison with the conventional inverter, the number of circuit components in the case of 7x step-up is compared, and this result showed that the proposed inverter can reduce 40 circuit components from the conventional inverter. In the theoretical analysis, the validity of the proposed inverter was clarified. By using the analyzed results, the output voltage and the power efficiency of the proposed inverter can be obtained without complex calculations, because handy theoretical formulas were obtained. In the simulation, the simulated results showed the performances and the effectiveness of the proposed inverter. Concretely, in the range from 2 to 100W, the proposed inverter can offer more than 80% efficiency. However, the output power range of the proposed inverter is smaller than that of the conventional inverter. In the experiments, the feasibility of the proposed inverter was verified. Concretely, the staircase AC waveform was clarified in practice by the experimental circuit built on a universal board. These results indicate as follows: (1) the proposed inverter has good characteristics as a DC-AC inverter and (2) its circuit size is much smaller than the conventional inverter.

The detailed experiments of the proposed inverter are left to a future study.

REFERENCES