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A MEDIAN FILTERING CIRCUIT USING CLOCKED CMOS NEURON INVERTERS FOR IMPLANTABLE ELECTRONIC MEDICAL DEVICES

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Abstract. *In the past few years, implantable electronic medical devices are receiving much attention in the field of biomedical engineering. In the design of the implantable electronic medical devices, not only small size but also low power consumption are required to achieve long working-life. In this paper, we present a complementary metal oxide semiconductor (CMOS) median filtering circuit using clocked neuron CMOS inverters. The aim of this work is to develop a CMOS implementable preprocessing circuit realizing low power consumption for implantable electronic medical devices such as a retinal prosthesis system. By controlling the duty cycle of clock pulses in the clocked neuron CMOS inverters, the proposed median filtering circuit can suppress the through current of inverters. Therefore, the proposed circuit can realize smaller power consumption than conventional median filtering circuits. Moreover, without arithmetic logic circuits, the median filtering based on the binary search algorithm is achieved in the proposed circuit. Therefore, the proposed circuit can offer the simple circuit configuration. Concerning the proposed circuit, the operation principle and theoretical design method are discussed in detail. Furthermore, the effectiveness of the proposed circuit is confirmed by simulation program with integrated circuit emphasis (SPICE) simulations. The simulated results demonstrate that the proposed median filtering circuit can reduce about 37% power consumption from the conventional circuit using CMOS neuron inverters.*
Keywords: Median filtering circuits, Neuron MOSFETs, Neuron CMOS inverters, Image processing, Implantable electronics

1. **Introduction.** To support damaged or missing biological structure, implantable electronic medical devices are receiving much attention in the past few years. Among others, the development of a retinal prosthesis system [1-3] is one of the most challenging issues to support partial or total blind patients. In the design of the implantable electronic medical devices, not only small size but also low power consumption are required, because the electronic devices are implanted within the body of a patient. To develop an efficient retinal prosthesis system realizing long working-life, we focused on the median filtering circuit which is one of the most popular preprocessing circuits.

In the field of image processing, the median filter is used to reduce the noise in an input image. In previous studies, many types of the median filtering techniques have been proposed [4-8]. For example, Boateng et al. suggested the improved median filtering technique to suppress impulse noise [4]. Rajasekaran et al. presented the median filtering technique utilizing Canny operator [5]. However, these software-based median filtering techniques are difficult to implement into an LSI chip. On the other hand, some researchers are trying to implement the median filter into an LSI chip. For example, Kalali and Hamzaoglu implemented an adaptive median filter into a field programmable gate array (FPGA) chip [6]. This circuit can realize low power consumption by using the low complexity 2D adaptive median filter algorithm. In the same way, the efficient medina filtering circuit can be implemented easily by employing embedded systems such as FPGA, Intel Edison, and Arduino. However, the hardware approach utilizing the embedded system is too bulky for implantable electronic medical devices. Moreover, due to the limitation of the number of electrodes implanted near retina, it is not necessary to process a high-resolution image in the retinal prosthesis system. Different from these approaches utilizing embedded systems, Lee and Jen developed a bit-level scalable median filter [7]. This median filtering circuit is suitable for IC implementation, because it can be designed using standard complementary metal oxide semiconductor (CMOS) technology. However, the circuit configuration of the circuit reported in [7] is complex, because it is designed by using voltage mode techniques. Following this study, Noisuwan et al., Hung et al., and Siskos suggested a simple CMOS median filter circuit design [8-10]. By using current mode techniques, the median filter circuits reported in [8-10] can offer a simple circuit configuration. However, this technique suffers from high power consumption. Furthermore, Muñiz-Montero et al. proposed a compact CMOS Class-AB analog median filter [11]. The layout area of the median filter circuit reported in [11] is saved by employing trans-conductance comparators accomplished with differential flipped voltage followers. However, this circuit still has high power consumption, because the differential flipped voltage followers require some current sources. To overcome this problem, Yamasaki and Shibata suggested a high-speed median filter using floating-gate-MOS-based low-power majority voting circuits [12]. Generally, it is known that the floating-gate MOS technology can achieve high-speed operation, small size, and low power consumption [13-16]. For example, Shen et al. and Inaba et al. suggested fundamental circuit components realizing a low voltage and low power, such as multi-valued logic circuits [14] and down literal circuits [15]. Likewise, Fukuhara and Yoshida developed a low power Hamming distance search CAM using neuron MOS transistors [16]. By using the floating-gate MOSFET [13] referred to as the neuron MOSFET [14-16], this median filtering circuit can offer not only high-speed operation but also low power consumption. However, in order to develop more efficient implantable circuit, there is still room for improvement in the point of power consumption.

To develop a CMOS implementable preprocessing circuit for implantable electronic medical devices such as a retinal prosthesis system, this paper proposes a CMOS median filtering circuit realizing low power consumption and simple circuit configuration. Unlike conventional circuits, the proposed circuit is designed by utilizing clocked neuron CMOS inverters. Therefore, the proposed circuit can achieve low power consumption, because the through current of CMOS inverters is suppressed by controlling the duty cycle of clock pulses of the clocked neuron CMOS inverters. Furthermore, the proposed circuit provides a simple circuit configuration by employing the binary search algorithm. Without arithmetic logic circuits, such as adder, and multiplier, the median filtering using the binary search algorithm can be implemented by using clocked neuron CMOS inverters. Concerning the proposed circuit, the operation principle and theoretical design method

are discussed in detail. Furthermore, the effectiveness of the proposed circuit is clarified by simulation program with integrated circuit emphasis (SPICE) simulations.

This paper is organized as follows: Section 2 gives the circuit configuration of the proposed CMOS median filter. Furthermore, the operation principle and theoretical design method are discussed in detail. Section 3 demonstrates the results of SPICE simulation to confirm the validity of circuit design, where the comparison concerning power consumption is performed between the proposed circuit and conventional median filtering circuits. Finally, Section 4 presents conclusion and future work of this study.

2. Circuit Configuration.

2.1. Operation principle.

To achieve small and simple circuit configuration, the operation principle of the proposed median filtering circuit is based on the binary search algorithm. From the input image of $m \times n$ pixels, the k-th ($k = 0, \ldots, N-1$) bit of the median value $M_i[k]$ ($i = 1, \ldots, m \times n$) is obtained as follows:

$$M_i[k] = \begin{cases} 1, & \text{if } \sum\limits_{j \in W} \frac{P_j[k]}{W} > 0.5 \\ 0, & \text{if } \sum\limits_{j \in W} \frac{P_j[k]}{W} \leq 0.5 \end{cases}, \tag{1}$$

where $P_j[k]$ ($= \{0, 1\}$) is a value of the k-th ($k = 0, \ldots, N-1$) bit of the j-th pixel and W is the window size of the median filter. As (1) shows, the median value $M_i[k]$ becomes "1" when the value of majority group is "1". On the other hand, the median value $M_i[k]$ becomes "0" when the value of majority group is "0". According to the median value $M_i[k]$ of the i-th pixel, the value of the i-th pixel $P_i[k]$ is changed as follows:

$$P_i[k-1] = \cdots = P_i[0] = \begin{cases} 1, & \text{if } P_i[k] \neq M_i[k] \text{ and } P_i[k] = 1 \\ 0, & \text{if } P_i[k] \neq M_i[k] \text{ and } P_i[k] = 0 \end{cases}. \tag{2}$$

By iterating the operation of (1) and (2) from $k = N-1$ to 0, the median value of P_i is derived.

To help readers' understanding, let us consider the median detection by using the example of Table 1. In this example, the window size W is 5, the bit-length N is 4, and the values of the input are $P_1 = \{1, 0, 0, 1\} = 9_{(10)}$, $P_2 = \{0, 1, 1, 1\} = 7_{(10)}$, $P_3 = \{1, 0, 1, 0\} = 10_{(10)}$, $P_4 = \{1, 1, 0, 0\} = 12_{(10)}$, and $P_5 = \{0, 1, 0, 0\} = 8_{(10)}$. The operation principle of the proposed medina filter is as follows. First, in the case of $k = 3$, the majority group is $P_1[3]$, $P_3[3]$, and $P_4[3]$. Therefore, we have $M_i[3] = 1$, because the majority is "1". On the other hand, the remaining bits of P_2 and P_5 are all changed to "0". Next, in the case of $k = 2$, the majority group is $P_1[2]$, $P_2[2]$, $P_3[2]$, and $P_5[2]$. Therefore, we have $M_i[2] = 0$, because the majority is "0". On the other hand, the remaining bits of P_4 are all changed to "1". In the same way, the median value $M_i[1]$ and $M_i[0]$ are obtained by iterating these processes. As you can see from Table 1, the median value $P_1 = \{1, 0, 0, 1\} = 9_{(10)}$ is detected by this operation principle.

2.2. Circuit design.

The block diagram of the proposed CMOS median filtering circuit is drawn in Figure 1. In the proposed circuit, the median detection is performed by a bit-comparison-based technique in order to realize small hardware size. The proposed circuit consists of N (= 2, 3, ...) majority circuits (MCs) and N (= 2, 3, ...) bit-comparators (BCs), where N is the number of bits and W is the window size. In Figure 1, the operation of the MC corresponds to (1). The MC is the W-inputs/1-output CMOS analog circuit designed by utilizing clocked neuron CMOS inverters. Usually, arithmetic logic circuits, such as adder, and multiplier, are necessary to implement (1) into a digital circuit. However, owing to the circuit design employing clocked neuron CMOS inverters,

TABLE 1. An example of the median detection

Window size $W = 5$	(MSB) $k = 3$	$k = 2$	$k = 1$	(LSB) $k = 0$
$P_1 = \{1, 0, 0, 1\}$ $(= 9_{(10)})$	$\{\boxed{1}, 0, 0, 1\}$ (Major)	$\{1, \boxed{0}, 0, 1\}$ (Major)	$\{1, 0, \boxed{0}, 1\}$ (Major)	$\{1, 0, 0, \boxed{1}\}$ (Major)
$P_2 = \{0, 1, 1, 1\}$ $(= 7_{(10)})$	$\{\boxed{0}, 0, 0, 0\}$ (Minor)	$\{0, \boxed{0}, 0, 0\}$ (Major)	$\{0, 0, \boxed{0}, 0\}$ (Major)	$\{0, 0, 0, \boxed{0}\}$ (Minor)
$P_3 = \{1, 0, 1, 0\}$ $(= 10_{(10)})$	$\{\boxed{1}, 0, 1, 0\}$ (Major)	$\{1, \boxed{0}, 1, 0\}$ (Major)	$\{1, 0, \boxed{1}, 1\}$ (Minor)	$\{1, 0, 1, \boxed{1}\}$ (Major)
$P_4 = \{1, 1, 0, 0\}$ $(= 12_{(10)})$	$\{\boxed{1}, 1, 0, 0\}$ (Major)	$\{1, \boxed{1}, 1, 1\}$ (Minor)	$\{1, 1, \boxed{1}, 1\}$ (Minor)	$\{1, 1, 1, \boxed{1}\}$ (Major)
$P_5 = \{0, 1, 0, 0\}$ $(= 8_{(10)})$	$\{\boxed{0}, 0, 0, 0\}$ (Minor)	$\{0, \boxed{0}, 0, 0\}$ (Major)	$\{0, 0, \boxed{0}, 0\}$ (Major)	$\{0, 0, 0, \boxed{0}\}$ (Minor)
Median value $M_{i,j}[k]$ $(\{1, 0, 0, 1\} = 9_{(10)})$	1	0	0	1

the proposed circuit can realize the operation in (1) without arithmetic logic circuits. On the other hand, the operation of the BC corresponds to (2), where the BC consists of W $(= 2, 3, \dots)$ logic circuits (LCs). The LC is the 4-inputs/3-outputs logic circuit. Unlike Equation (1), there is no arithmetic logic operations in (2). Therefore, the LC is designed by combinational logic circuits.

Figure 2 illustrates the LC in the bit-comparator (BC). In the LC of Figure 2, the following bit-comparison is performed:

$$L_i[k] = S0_i[k] \cdot S1_i[k] + P_i[k] \cdot \overline{S1_i[k]}, \tag{3}$$

where

$$S0_i[k-1] = S0_i[k] \cdot S1_i[k] + \overline{M_i[k]} \cdot \overline{S1_i[k]} \cdot P_i[k] \tag{4}$$

and

$$S1_i[k-1] = M_i[k] \oplus P_i[k] + S1_i[k]. \tag{5}$$

In (3)-(5), $M_i[k]$ is the k-th bit of the median output and $L_i[k]$ is the k-th bit of the BC output. To achieve the median detection using the bit-comparison-based technique, $S0_i[k-1]$ and $S1_i[k-1]$ are inputted to the $(k-1)$-th LC and $L_i[k]$ is inputted to the MC. In the MC, the majority of $L_i[k]$ is detected by using clocked neuron CMOS inverters.

The circuit configuration of the proposed majority circuit using a clocked neuron CMOS inverter is shown in Figure 3, where C_p denotes the parasitic capacitance and Φ denotes the non-overlapped two-phase clock pulse. While the clock Φ is in a high level, the clocked neuron CMOS inverter behaves as a traditional neuron CMOS inverter [17-20]. In this case, the drain currents in saturation region, I_{dp} and I_{dn}, are given by

$$|I_{dp}| = \frac{1}{2}\mu_p C_{ox} \frac{W_p}{L_p} \left(V_{GS} - |V_{THp}|\right)^2 \tag{6}$$

and

$$I_{dn} = \frac{1}{2}\mu_n C_{ox} \frac{W_n}{L_n} \left(V_{GS} - V_{THn}\right)^2, \tag{7}$$

where μ_p and μ_n are the effective mobility of holes and electrons, C_{ox} is the gate capacitance per unit area, W_p and W_n are the gate width of PMOS and NMOS, L_p and L_n

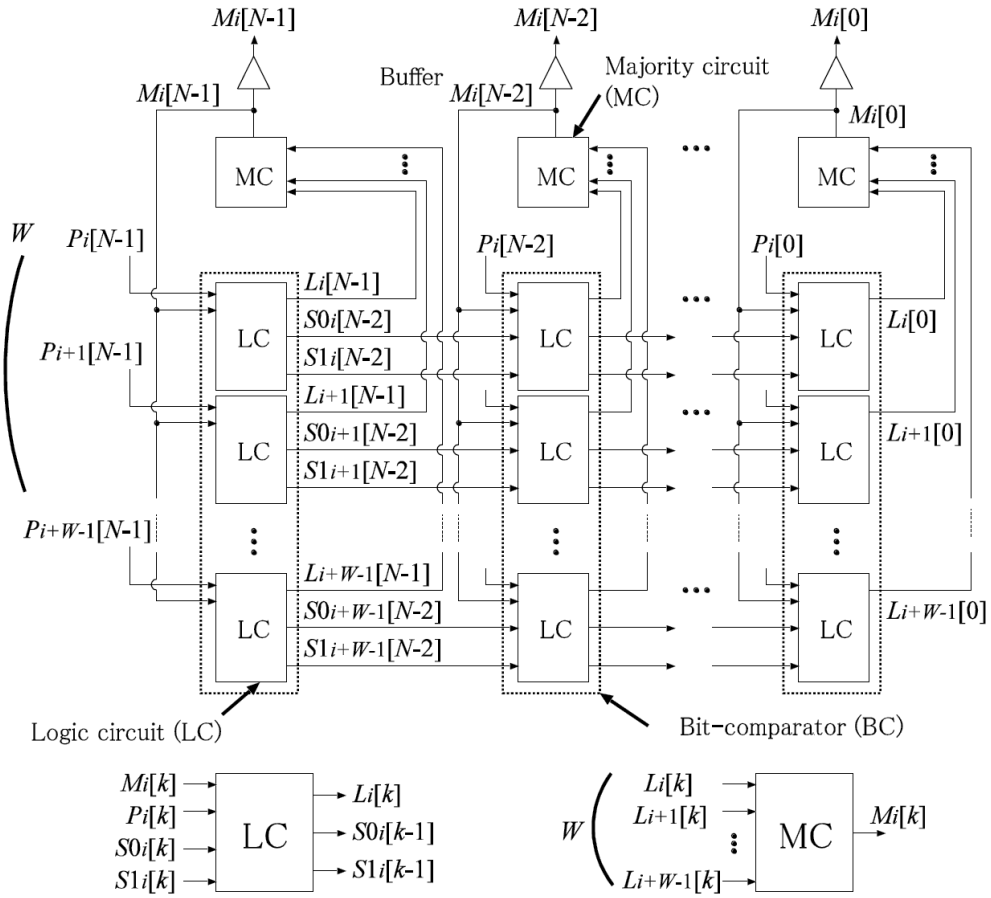

FIGURE 1. Block diagram of CMOS median filter

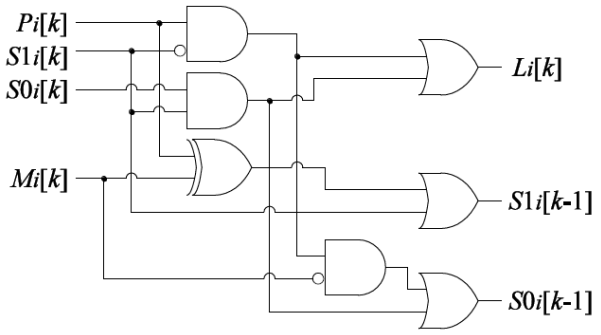

FIGURE 2. Block diagram of a logic circuit

are the gate lengths of PMOS and NMOS, V_{THp} and V_{THn} are the threshold voltages of PMOS and NMOS, and V_{GS} is the voltage between gate terminal and source terminal. In (6) and (7), the channel-length-modulation of transistors is not taken into account to simplify the theoretical analysis. When the clock Φ is in a high level, the floating gate voltage $V_{Fi}[k]$ of the clocked neuron inverter is given by

$$V_{Fi}[k] = \frac{\sum_{j \in W} L_j[k] C_u + V_{dd} C_{FN}}{W C_u + C_{FP} + C_{FN}}, \tag{8}$$

where C_u is a unit capacitance between an input terminal and the floating gate, C_{FN} is a capacitance between the floating gate and N-type region, and C_{FP} is a capacitance

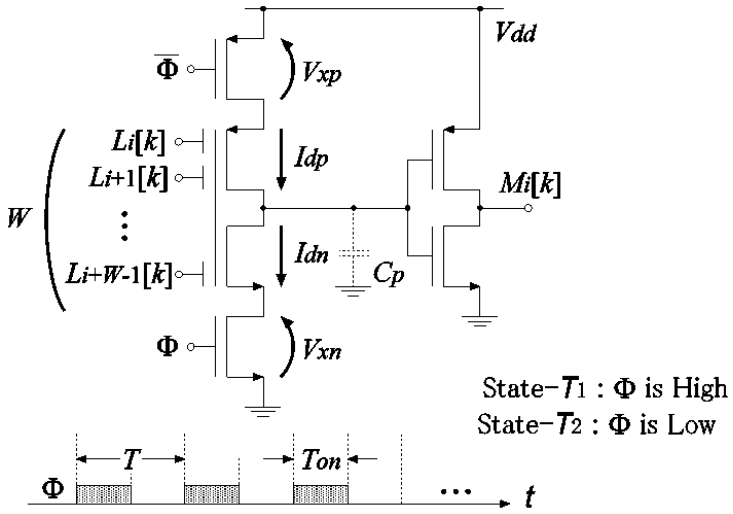

FIGURE 3. Majority circuit using a clocked neuron CMOS inverter

between the floating gate and P-type region. In the proposed median filter, the unit capacitance C_u is designed to satisfy the following conditions:

$$C_u >> C_{FN} \text{ and } C_{FP} = C_{FN}. \tag{9}$$

From (9), the floating gate voltage $V_{Fi}[k]$ can be rewritten as

$$V_{Fi}[k] \cong \sum_{j \in W} \frac{L_j[k]}{W}, \tag{10}$$

where

$$\sum_{j \in W} L_j[k] \in \{0, V_{dd}, 2V_{dd}, \ldots, WV_{dd}\}. \tag{11}$$

Using (10), the drain currents (6) and (7) can be rewritten as

$$|I_{dp}| = \frac{1}{2}\mu_p C_{ox} \frac{W_p}{L_p} \left(V_{dd} - V_{xp} - \sum_{j \in W} \frac{L_j[k]}{W} - |V_{THp}| \right)^2 \tag{12}$$

and

$$I_{dn} = \frac{1}{2}\mu_n C_{ox} \frac{W_n}{L_n} \left(\sum_{j \in W} \frac{L_j[k]}{W} - V_{xn} - V_{THn} \right)^2. \tag{13}$$

In the switching threshold, (12) is equal to (13), because both the PMOS and NMOS transistors are in saturation. Therefore, assuming the following conditions:

$$V_{xp} = V_{xn} \text{ and } \sqrt{\mu_n C_{ox} \frac{W_n}{L_n}} = \sqrt{\mu_p C_{ox} \frac{W_p}{L_p}}, \tag{14}$$

we have the switching threshold of the clocked CMOS neuron inverter as

$$\sum_{j \in W} L_j[k] = \frac{WV_{dd}}{2}. \tag{15}$$

From (15), $M_i[k]$ can be obtained as

$$M_i[k] = \begin{cases} V_{dd}, & \text{if } \sum\limits_{j \in W} L_j[k] \le \frac{WV_{dd}}{2} \\ 0, & \text{if } \sum\limits_{j \in W} L_j[k] > \frac{WV_{dd}}{2} \end{cases}. \tag{16}$$

As you can see from (1) and (16), the clocked neuron inverter behaves as a majority circuit when the clock Φ is in a high level.

While the clock Φ is in a high level, the output of the clock neuron CMOS inverter is charged in C_p. On the other hand, the clocked neuron inverter becomes high-impedance when the clock Φ is in a low level, because the clock neuron CMOS inverter is not connected between the power source and ground. In this timing, the output held in C_p is supplied to the gate terminal of the CMOS inverter. That is to say, the proposed majority circuit behaves like a sample-and-hold circuit, where State-T_1 and State-T_2 correspond to the holding process and the sampling processes, respectively. By adjusting the duty cycle of clock pulses, the proposed median filter can reduce power consumption, because the through current of the neuron inverter is suppressed owing to this technique. Of course, we can design other preprocessing circuits realizing low power consumption by modifying the proposed majority circuit shown in Figure 3. As an example, the binarizing and resizing circuit realizing low power consumption will be described in Appendix.

3. **Simulation.** The validity of the circuit design and the effectiveness of the proposed median filter are clarified by SPICE simulations. In this simulation, the proposed median filter with 3-bits/3-inputs was implemented by assuming 0.35μm CMOS process.

Figure 4 demonstrates the simulated output of the proposed median filtering circuit, where the input voltages of the proposed median filter, P_1, P_2, and P_3, are as shown in Table 2. In Figure 4, the supply voltage V_{dd}, the duty cycle D, and the period of clock pulse T were set to 1.8V, 0.5, and 0.1μs, respectively. As you can see from Figure 4 and Table 2, the proposed median filter can detect the median value M_i from P_1, P_2, and P_3. Concretely, the output $M_i = \{5, 2, 5\}$ was derived from $P_1 = \{6, 1, 6\}$, $P_2 = \{5, 2, 5\}$, and $P_3 = \{3, 4, 3\}$.

The power consumption of the proposed median filtering circuit is demonstrated in Figure 5, where the power consumption of the proposed circuit is compared with that of conventional median filtering circuits [7,12]. In Figure 5, the blue-line shows the power consumption of the proposed median filter, the orange-line shows the power consumption of the conventional median filter using floating-gate-MOS-based low-power majority voting circuits [12], and the grey line shows the conventional median filter using CMOS majority circuits [7] shown in Figure 6. As Figure 5 shows, the proposed median filter can achieve the smallest power consumption. Concretely, more than 37% power consumption can be reduced from the conventional circuit using neuron CMOS inverters [12] when the duty cycle is 0.5.

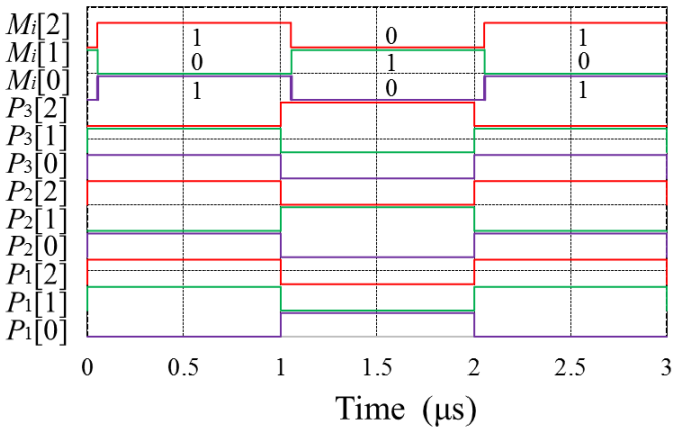

FIGURE 4. Simulated output of the proposed median filter

TABLE 2. Setting of SPICE simulation

Time (μs)	0 – 1.0	1.0 – 2.0	2.0 – 3.0
Input	Value		
P_1	$\{V_{dd}, V_{dd}, 0\}$ $(\{1,1,0\} = 6_{(10)})$	$\{0, 0, V_{dd}\}$ $(\{0,0,1\} = 1_{(10)})$	$\{V_{dd}, V_{dd}, 0\}$ $(\{1,1,0\} = 6_{(10)})$
P_2	$\{V_{dd}, 0, V_{dd}\}$ $(\{1,0,1\} = 5_{(10)})$	$\{0, V_{dd}, 0\}$ $(\{0,1,0\} = 2_{(10)})$	$\{V_{dd}, 0, V_{dd}\}$ $(\{1,0,1\} = 5_{(10)})$
P_3	$\{0, V_{dd}, V_{dd}\}$ $(\{0,1,1\} = 3_{(10)})$	$\{V_{dd}, 0, 0\}$ $(\{1,0,0\} = 4_{(10)})$	$\{0, V_{dd}, V_{dd}\}$ $(\{0,1,1\} = 3_{(10)})$
Output	Value		
M_i	$\{V_{dd}, 0, V_{dd}\}$ $(\{1,0,1\} = 5_{(10)})$	$\{0, V_{dd}, 0\}$ $(\{0,1,0\} = 2_{(10)})$	$\{V_{dd}, 0, V_{dd}\}$ $(\{1,0,1\} = 5_{(10)})$

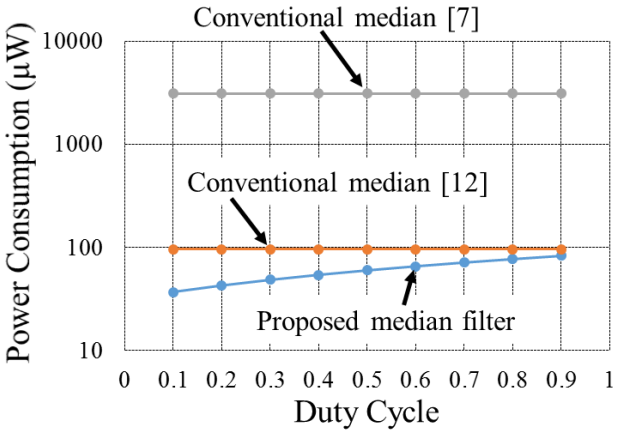

FIGURE 5. Simulated power consumption of the median filter

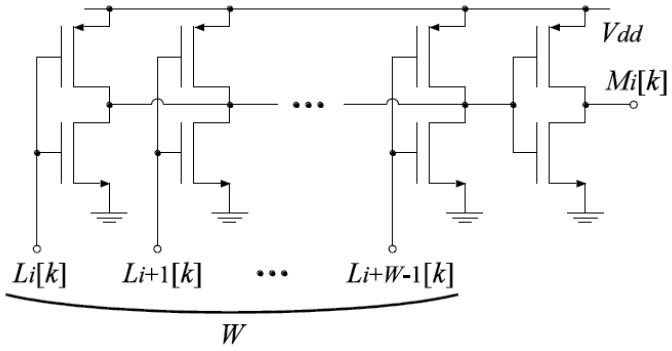

FIGURE 6. Conventional CMOS majority circuit [7]

Furthermore, the proposed median filter can improve power consumption by reducing the duty cycle D. Of course, the setting of duty cycle depends on the response speed of CMOS transistors. Table 3 shows the comparison of the number of circuit components for the majority circuits in median filters. As Figure 6 and Table 3 show, the conventional circuit can realize simple circuit configuration by series-connecting CMOS inverters. However, the circuit complexity of the proposed circuit is almost the same as that of conventional circuits.

TABLE 3. Number of circuit components for majority circuits

	Number of circuit components		
	MOSFETs	Neuron inverters	Capacitors
Proposed majority circuit	4	1	1
Conventional majority circuit [7]	8	0	0
Conventional majority circuit [12]	2	1	1

4. **Conclusions.** For implantable electronic medical devices, a CMOS median filtering circuit using clocked neuron CMOS inverters has been proposed in this paper. The feature of the proposed median filtering circuit is the design for simple circuit configuration and low power consumption using clocked neuron CMOS inverters. Concerning the proposed circuit, the operation principle and theoretical design method were discussed in detail. Furthermore, SPICE simulations confirmed the effectiveness of the proposed circuit.

The SPICE simulations showed the following results: 1). by using clocked neuron CMOS inverters, the proposed median filter with 3-bits/3-inputs offered median values without arithmetic logic circuits; and 2). when the duty cycle is 0.5, the proposed circuit reduced about 37% power consumption from the conventional median filter using floating-gate-MOS-based majority voting circuits. Furthermore, the proposed median filter can improve power consumption further by reducing the duty cycle D. From these results, the proposed circuit can realize not only simple circuit configuration but also small power consumption. The proposed circuit will open up a new vista for the implantable electronic medical devices realizing long working-life.

In a future study, we are going to implement the proposed circuit into an IC chip. The test evaluation is performed concerning the performance of the IC chip, such as layout area, power consumption and response speed.

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Appendix.

A.1. **Binarizing and Resizing Circuit.** As an application of the proposed majority circuit, we present the binarizing and resizing circuit using a clocked neuron CMOS inverter in this Appendix. In the binarizing and resizing circuit, the following operation is performed in order to obtain the pixel value of the resized image, B_i $(i = 1, \ldots, m' \times n')$, from the input image of $m \times n$ pixels:

$$B_i = \begin{cases} 1, & \text{if } \dfrac{\sum\limits_{j \in W'} \sum\limits_{l=1}^{N} P_j[N-l] \cdot 2^{N-l}}{\sum\limits_{j \in W'} \sum\limits_{l=1}^{N} 2^{N-l}} > 0.5 \\ 0, & \text{if } \dfrac{\sum\limits_{j \in W'} \sum\limits_{l=1}^{N} P_j[N-l] \cdot 2^{N-l}}{\sum\limits_{j \in W'} \sum\limits_{l=1}^{N} 2^{N-l}} \leq 0.5 \end{cases}, \tag{17}$$

where W' is the window size to resize the input image. The size of the resized image is defined as

$$m' = \frac{m}{W'} \text{ and } n' = \frac{n}{W'}. \tag{18}$$

Figure 7 illustrates the circuit configuration of the binarizing and resizing circuit, where the floating gate capacitance is set to $2^{N-1-k} \times C_u$ for $P_i[k]$. As you can see from Figures 3 and 7, the circuit configuration of the majority circuit of the median filtering circuit and the binarizing and resizing circuit is almost the same. By modifying the capacitor size of the clocked neuron CMOS inverter in the majority circuit, we can design the binarizing and resizing circuit of Figure 7. In Figure 7, the arithmetic operation in (17) is realized by the binary-weighted floating capacitances, where the capacitor size is set to $2^{N-l}C_u$ for

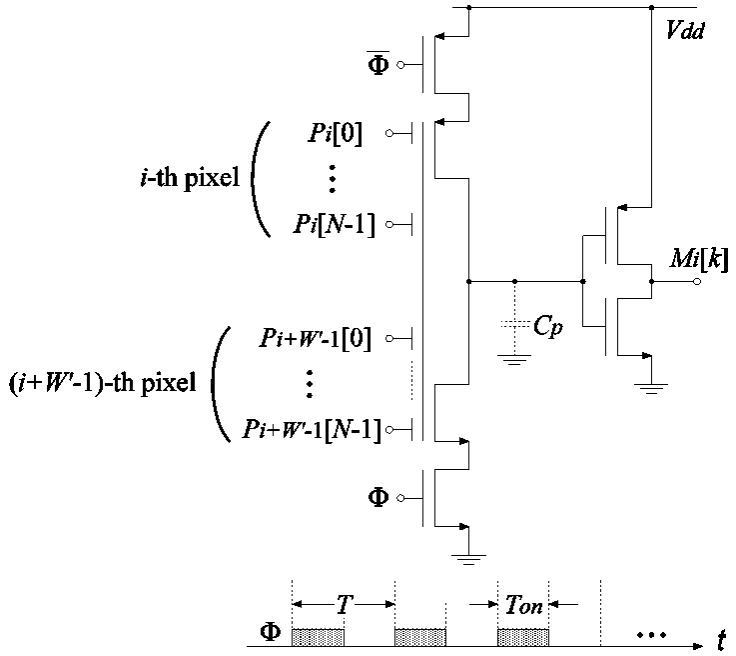

FIGURE 7. Binarizing and resizing circuit using a clocked neuron CMOS inverter

the $(N-l)$-th bit of the input pixel. Owing to the binary-weighted floating capacitances, the proposed circuit can achieve simple circuit configuration as shown in Figure 7. The binarizing and resizing circuit also requires no arithmetic logic circuit.

In Figure 7, the floating gate voltage V_{FBi} of the clocked neuron inverter is given by

$$V_{FBi} = \frac{\sum\limits_{j\in W'}\sum\limits_{l=1}^{N} C_u P_j[N-l]\cdot 2^{N-l} + V_{dd}C_{FN}}{\sum\limits_{j\in W'}\sum\limits_{l=1}^{N} 2^{N-l}C_u + C_{FP} + C_{FN}}, \tag{19}$$

where the unit capacitance C_u satisfies the condition of (9). Using (9), the floating gate voltage (19) can be rewritten as

$$V_{FBi} = \frac{\sum\limits_{j\in W'}\sum\limits_{l=1}^{N} P_j[N-l]\cdot 2^{N-l}}{\sum\limits_{l=1}^{N} 2^{N-l}W'}, \tag{20}$$

where

$$P_j[k] \in \{0, V_{dd}\}. \tag{21}$$

From (20) and (21), we get the pixel value of the resized image as follows:

$$B_i = \begin{cases} 0, & \text{if } \dfrac{\sum\limits_{j\in W'}\sum\limits_{l=1}^{N} P_j[N-l]\cdot 2^{N-l}}{\sum\limits_{l=1}^{N} 2^{N-l}W'} \le \dfrac{V_{dd}}{2} \\ V_{dd}, & \text{if } \dfrac{\sum\limits_{j\in W'}\sum\limits_{l=1}^{N} P_j[N-l]\cdot 2^{N-l}}{\sum\limits_{l=1}^{N} 2^{N-l}W'} > \dfrac{V_{dd}}{2} \end{cases}. \tag{22}$$

As you can see from (22), the binarizing and resizing circuit of Figure 7 can realize binarizing and resizing operations. Furthermore, the reduction of power consumption can

be achieved by controlling the clocked neuron inverter. Of course, the proposed median filter is not suitable for the application systems that require high-speed operation, because the clocked neuron inverter requires clock pulses to achieve low power consumption.

A.2. **Simulated Result.** To clarify the characteristics of the binarizing and resizing circuit using a clocked neuron CMOS inverter, SPICE simulations were performed concerning the 4-bits/4-inputs circuit. In the SPICE simulations, the input voltages, P_1, P_2, P_3 and P_4, were set as shown in Table 4.

TABLE 4. Setting of SPICE simulation

Time (μs)	0 | 0.5	0.5 | 1.0	1.0 | 1.5	1.5 | 2.0	2.0 | 2.5	2.5 | 3.0	3.0 | 3.5	3.5 | 4.0	4.0 | 4.5
Input	Value								
P_1	15	7	11	3	13	5	9	1	14
P_2	15	14	7	6	11	10	3	2	13
P_3	15	13	14	12	7	5	6	4	11
P_4	15	11	13	9	14	10	12	8	7
Output	Value								
B_i	V_{dd}	V_{dd}	V_{dd}	0	V_{dd}	0	0	0	V_{dd}

Figure 8 demonstrates the simulated outputs of 4-bits/4-inputs circuit, where the supply voltage V_{dd}, the duty cycle D, and the period of clock pulse T were set to 1.8V, 0.5, and 0.1μs, respectively. As you can see from Figure 8 and Table 4, the proposed binarizing circuit can offer the pixel value of the resized image, B_i. Figure 9 demonstrates the power consumption of the binarizing and resizing circuit as a function of the duty cycle. In Figure 9, the blue-line shows the power consumption of the binarizing and resizing circuit using a clocked neuron CMOS inverter and the orange-line shows the power consumption of the binarizing and resizing circuit without a clocked neuron CMOS inverter. In Figure 9, the binarizing and resizing circuit using a clocked neuron CMOS inverter can reduce more than 43% power consumption when the duty cycle is 0.5. As Figures 8 and 9 show, the binarizing and resizing circuit realizing low power consumption can be designed by modifying the proposed majority circuit.

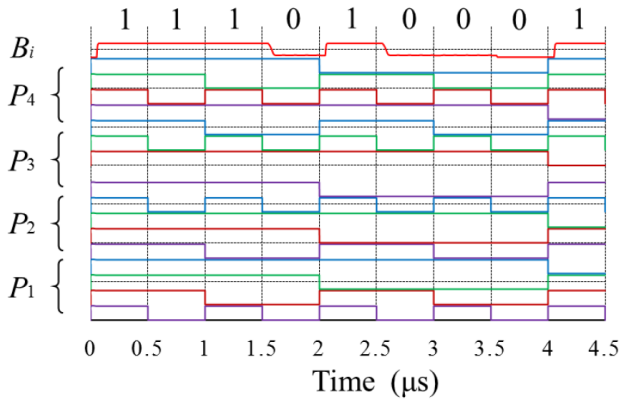

FIGURE 8. Simulated output of the proposed median filter

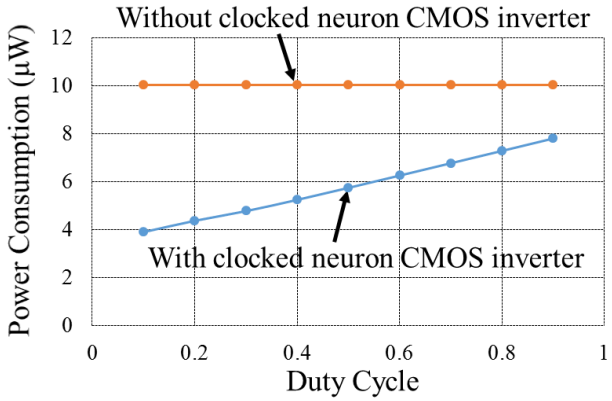

FIGURE 9. Simulated power consumption of the median filter