International Journal of Innovative
Computing, Information and Control
Volume **13**, Number **4**, August **2017**

 ISSN 1349-4198
pp. **1369–1384**

# DESIGN OF A NESTING-TYPE SWITCHED-CAPACITOR AC/DC CONVERTER USING VOLTAGE EQUALIZERS

Kei Eguchi[1], Tipparat Junsing[2], Amphawan Julsereewong[2]
Wanglok Do[1] and Ichirou Oota[3]

[1]Department of Information Electronics
Fukuoka Institute of Technology
3-30-1 Wajirohigashi, Higashi-ku, Fukuoka 811-0295, Japan
eguti@fit.ac.jp; dwl12345@naver.com

[2]Faculty of Engineering
King Mongkut's Institute of Technology Ladkrabang
Ladkrabang, Bangkok 10520, Thailand
juryying@hotmail.com; amphawan.ju@kmitl.ac.th

[3]Department of Information, Communication and Electronics Engineering
National Institute of Technology, Kumamoto College
2659-2 Suya, Koushi, Kumamoto 861-1102, Japan
oota-i@kumamoto-nct.ac.jp

Received February 2017; revised May 2017

Abstract. *For electric appliances, an electric circuit that changes an alternating current (ac) into a direct current (dc) is necessary. Among others, a small and light ac/dc converter is indispensable to develop novel mobile devices. As one of the most promising design approaches, the ac/dc converter designed by switched-capacitor (SC) techniques attracts many researchers' attention, because the SC ac/dc converter can be implemented without a high turn ratio transformer. Owing to the heavy transformer-less design, the SC ac/dc converter can realize smaller size and lighter weight than traditional ac/dc converters. However, the SC ac/dc converter suffers from complexity of the circuit control and the inflexibility of conversion ratio. To overcome these problems, this paper proposes a nesting-type SC ac/dc converter using voltage equalizers. Unlike conventional SC ac/dc converters, the proposed converter consists of a full waveform rectifier with a big capacitor and nested voltage equalizers. In the nested voltage equalizers, a part of the capacitor voltage of a voltage equalizer is converted by other voltage equalizers, where each voltage equalizer is controlled by non-overlapped two-phase clock pulses. By the nesting conversion, the conversion ratio of the proposed converter is expressed as a reverse value of the total sum of main capacitors' voltage ratios. Therefore, the proposed converter can achieve not only simple circuit control but also flexible conversion ratios. Concerning the* $1/9\times$ *step-down SC ac/dc converter, the advantages of the proposed converter were investigated by theoretical analysis, simulated program with integrated circuit emphasis (SPICE) simulations, and experiments. First, mathematical formulas for estimating the characteristics of the proposed converter were derived theoretically by utilizing a simple four equivalent circuit. Then, by comparing the proposed converter with conventional SC ac/dc converters, the effectiveness of the proposed converter was clarified by SPICE simulations. Finally, the feasibility of the proposed converter was confirmed by using the experimental circuit implemented on a breadboard.*

**Keywords:** Ac/dc converters, Nesting conversion, Switched-capacitor circuits, Inductorless circuits, Voltage equalizers

1. **Introduction.** For electric appliances, an electric circuit that changes an alternating current (ac) into a direct current (dc) is a vital component. Among others, a small

and light ac/dc converter is indispensable to develop novel mobile devices. In general, the ac/dc converter has been implemented by using a high turn ratio transformer. The traditional ac/dc converter is useful for high and middle power applications, though the magnetic components in these converters are heavy and bulky. However, due to the existence of magnetic components, these traditional approaches are difficult to realize small and light converter.

As one of the most promising design approaches, the switched-capacitor (SC) technique [1-17] has been receiving much attention in order to design small and light ac/dc converters [1-12]. Although the SC ac/dc converter is not suitable for high power applications, the SC ac/dc converter can be implemented without a high turn ratio transformer. Therefore, the SC ac/dc converter can realize smaller size and lighter weight than traditional ac/dc converters. Over the past few decades, the study of the SC ac/dc converter has been tackled to design small and light converters. In 1989, the first SC ac/dc converter was proposed by Oota et al. [1]. By using multi-phase clock pulses, a part of the voltage stored in capacitors is provided as an output voltage one by one. Owing to the bidirectional converter topology, Oota's converter can achieve step-up/step-down ac/dc conversion. Based on this study, Oota et al. suggested the series-parallel type ac/dc converter [2] and its control method [3]. The series-parallel type converter can improve power efficiency for the 1st ac/dc converter. However, due to the slow switching control, the ripple noise of these converters is large. To overcome this problem, we proposed a high-speed control method for the series-parallel type ac/dc converter [4]. By using the high-speed control technique [4], the ripple noise of the series-parallel type ac/dc converter was reduced. However, this technique suffers from the complex switching control. Following this study, Oota et al. developed the differential SC ac/dc converter [5]. In the differential SC ac/dc converter, the differential voltage of two inputs is provided to an output load. However, the differential SC ac/dc converter requires two types of inputs. Apart from these converter topologies, Hara et al. and Terada et al. developed the ring-type ac/dc converter [6-9]. Unlike the series-parallel type ac/dc converter, the ring-type ac/dc converter can offer not only small inrush current but also flexible conversion ratios. Following these studies, Hirakawa et al. proposed the digital-selecting type ac/dc converter [10]. Unlike the ring-type converter and the series-parallel type converter, the voltage ratio of capacitors is set to powers of 2 in the digital-selecting type ac/dc converter. For this reason, the digital-selecting type ac/dc converter can achieve more flexible conversion ratio than the ring-type converter. However, many circuit components are necessary to implement these ac/dc converters. Furthermore, the switching control for the ring-type ac/dc converter and the digital-selecting type converter is complex, because the conversion ratio must be changed according to the amplitude of an ac input. To achieve simple switching control and small number of circuit components, Abe et al. proposed the series-connected ac/dc converter [11] and its improved topology [12]. By connecting voltage equalizers [13-15] in series, a high step-down conversion ratio is realized with small number of circuit components. Furthermore, the series-connected ac/dc converter [12] requires only two-phase clock pulses for ac/dc conversion. Therefore, the series-connected ac/dc converter [12] offers not only small size but also simple switching control. However, there is still room for improvement. The series-connected ac/dc converter can provide only the conversion ratios expressed by the multiplication form of conversion ratios of voltage equalizers. Therefore, the application field of the series-connected ac/dc converter is limited due to the inflexible conversion ratio. Of course, other converter topologies for dc/dc converters [16-18] have been proposed in past studies. However, these topologies cannot be applied for the SC ac/dc converter.

In this paper, we propose a nesting-type SC ac/dc converter in order to offer flexible conversion ratio and simple circuit control. Unlike conventional SC ac/dc converters, the proposed converter consists of a full waveform rectifier with a big capacitor and nested voltage equalizers. By nesting the voltage equalizers, the proposed converter converts a part of the capacitor voltage of a voltage equalizer by other voltage equalizers. By the nesting conversion, the conversion ratio of the proposed converter is expressed as a reverse value of the total sum of main capacitors' voltage ratios. In addition, the proposed topology can reduce the number of circuit components, because the voltage ratio of main capacitors is not equal by the nesting conversion. Therefore, the proposed converter realizing nesting conversion can offer not only flexible conversion ratios but also small number of circuit components. Furthermore, as reported in [13-15], the voltage equalizer is operated by non-overlapped two-phase clock pulses. Therefore, the proposed converter using nested voltage equalizers can achieve simple circuit control.

Concerning the proposed converter realizing the 1/9× step-down conversion, we conduct theoretical analysis, simulated program with integrated circuit emphasis (SPICE) simulations, and experiments. First, to estimate the circuit characteristics, a simple four equivalent circuit of the proposed converter is derived theoretically. Then, by using the SPICE simulator, the characteristic of the proposed converter is compared with that of conventional converters. Finally, to confirm the feasibility of the proposed circuit, experiments are performed by using the experimental circuit implemented on a breadboard.

The rest of this paper is as follows. In Section 2, the difference between the proposed topology and conventional topology [12] is discussed in detail in order to show the originality of the proposed topology. In Section 3, the equivalent model of the proposed converter is obtained theoretically to clarify the design condition of the proposed converter. Sections 4 and 5 describe the SPICE simulated results and experimental results to demonstrate the effectiveness of the proposed converter. Finally, the results of this study are summarized in Section 6.

## 2. **Circuit Configuration.**

### 2.1. **Conventional SC ac/dc converter.**

As an example of conventional SC ac/dc converters, the circuit configuration and the operation principle of the conventional ac/dc converter with double conversion topology [12] are discussed in this section. Figure 1 depicts the circuit configuration of the conventional series-connected converter reported in [12]. The conventional converter of Figure 1 is composed of a full bridge circuit with a big capacitor and two voltage equalizers, where 12 power switches, 11 capacitors, and 4 diodes are used. In the voltage equalizer, the main capacitors $C_{k,3}$, $C_{k,4}$ and $C_{k,5}$ ($k = \{1, 2\}$) work as a capacitive voltage divider, where electric charges stored in these capacitors are equalized by using non-overlapped two-phase clock pulses. Concretely, in State-$T_1$, the flying capacitors $C_{k,1}$ and $C_{k,2}$ are connected to the main capacitors $C_{k,3}$ and $C_{k,4}$ in parallel. Next, in State-$T_2$, $C_{k,1}$ and $C_{k,2}$ are connected to the main capacitors $C_{k,4}$ and $C_{k,5}$ in parallel. By repeating these processes, each voltage equalizer equalizes the electric charges of $C_{k,3}$, $C_{k,4}$ and $C_{k,5}$. Thus, the 1/3× step-down conversion is realized by each voltage equalizer. By connecting these voltage equalizers in series, the output voltage $V_{o2}$ becomes

$$V_{o2} = \left(\frac{1}{3} \times \frac{1}{3}\right) V_i = V_{o1} \times \left(\frac{1}{3}\right) V_i = \frac{1}{9} V_{i1}, \tag{1}$$

where $V_{i1}$ is the output voltage of the full bridge circuit, $V_{o1}$ ($= V_{i2}$) is the output voltage of the voltage equalizer-1, and $V_o$ ($= V_{o2}$) is the output voltage of the voltage equalizer-2. As (1) shows, the conversion ratio of the conventional converter is expressed by the

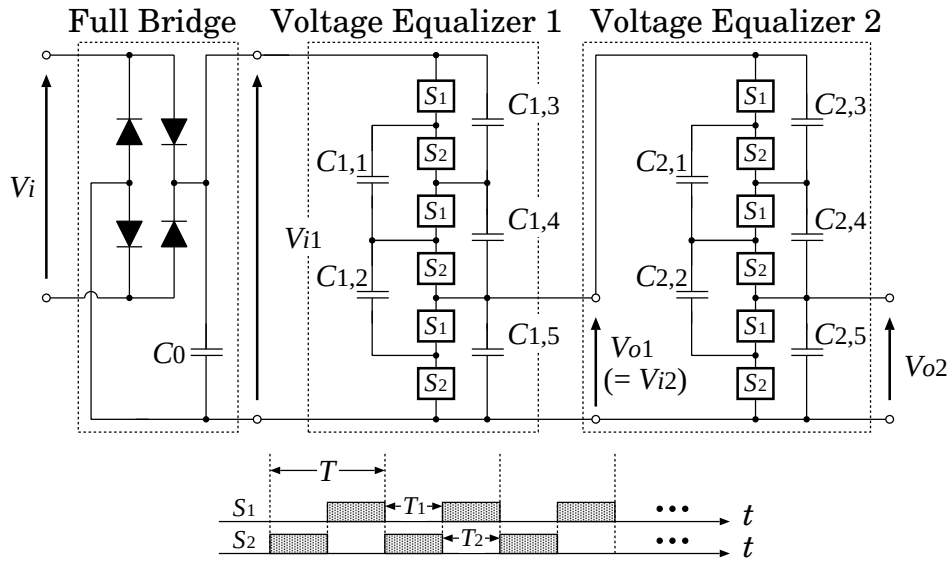


FIGURE 1. Conventional SC ac/dc converter proposed in [12]

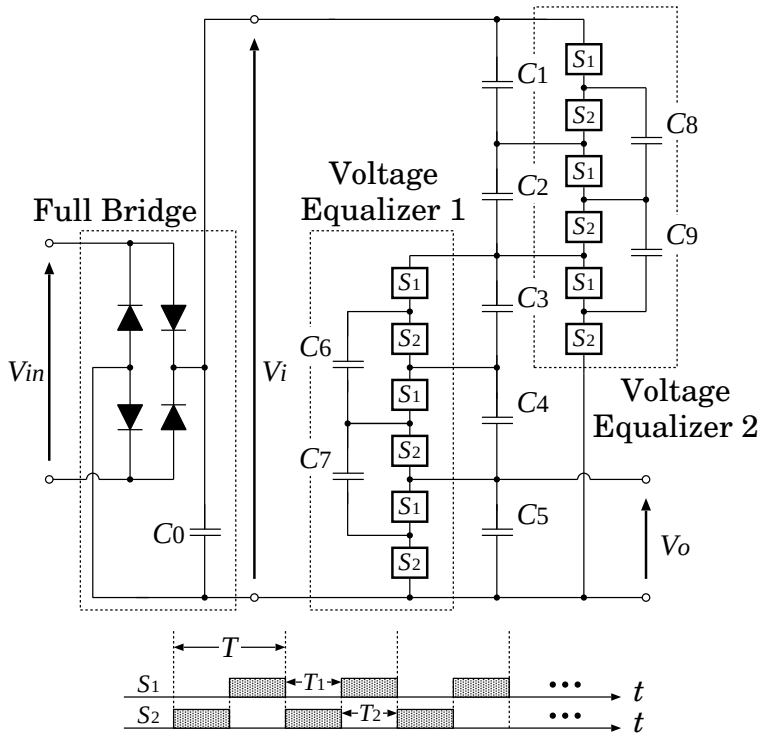


FIGURE 2. Proposed SC ac/dc converter realizing the 1/9× step-down conversion

multiplication form of conversion ratios of voltage equalizers. Hence, the conventional converter is difficult to realize flexible conversion ratio. For example, the series-connected converter cannot offer the conversion ratios of the prime number.

2.2. **Proposed SC ac/dc converter.** Figure 2 illustrates an example of the circuit configuration of the proposed SC ac/dc converter. In Figure 2, $C_k$ $(k = 1, \ldots, 5)$ is a main capacitor, $C_j$ $(j = 6, \ldots, 9)$ is a flying capacitor, $C_0$ is a smoothing capacitor, $V_{in}$ is an ac input, $V_o$ is a dc output, and $T$ is a period of clock pulses. As Figure 2 shows, the

proposed converter consists of a full waveform rectifier with a big capacitor and nested voltage equalizers. In the nested voltage equalizers, a part of the capacitor voltage of the voltage equalizer-1 is converted by the voltage equalizer-2, where each voltage equalizer is controlled by non-overlapped two-phase clock pulses. Concretely, in the voltage equalizer-1, the flying capacitors $C_6$ and $C_7$ are connected to the main capacitors $C_3$ and $C_4$ in State-$T_1$. In this timing, the voltage of $C_3$ becomes the same as that of $C_4$. Next, $C_6$ and $C_7$ are connected to the main capacitors $C_4$ and $C_5$ in State-$T_2$. In this timing, the voltage of $C_4$ becomes the same as that of $C_5$. Therefore, the voltage ratio of capacitors $C_3$, $C_4$, and $C_5$ becomes $1 : 1 : 1$. Similarly, in the voltage equalizer-2, the flying capacitors $C_8$ and $C_9$ are connected to the main capacitors $C_1$ and $C_2$ in State-$T_1$. In this timing, the voltage of $C_1$ becomes the same as that of $C_2$. Next, in State-$T_2$, the flying capacitors $C_8$ and $C_9$ are connected to the capacitors $C_2$ and the series-connected capacitors $C_3$, $C_4$, and $C_5$, respectively. In this timing, the voltage of $C_2$ becomes the same as that of the series-connected capacitors $C_3$, $C_4$, and $C_5$. By repeating these processes, the voltage ratio of capacitors $C_1$, $C_2$, $C_3$, $C_4$, and $C_5$ becomes $3 : 3 : 1 : 1 : 1$. Thus, the output voltage $V_o$ becomes

$$V_o = \frac{V_{C5}}{\sum_{k=1}^{5} V_{Ck}} \times V_i = \frac{V_{C5}}{V_{C5}(3+3+1+1+1)} \times V_i = \frac{1}{9} V_i, \tag{2}$$

where $V_{Ck}$ denotes the voltage of the $k$-th capacitor. Unlike the conventional SC ac/dc converter [12], the conversion ratio of the proposed converter is expressed as a reverse value of the total sum of $V_{Ck}$ ratios. For this reason, the proposed converter can achieve not only simple circuit control but also flexible conversion ratios. Of course, the proposed converter can provide other conversion ratios by combining voltage equalizers. In Appendix, the proposed converter realizing the $1/7\times$ step-down conversion will be described.

3. **Theoretical Analysis.** In this section, by deriving a simple equivalent circuit of the proposed converter, the characteristics, such as power efficiency and output voltage, of the proposed converter are clarified theoretically. To derive the equivalent circuit of the proposed converter, we employ a four-terminal equivalent model reported in [16-18]. Figure 3 illustrates the four-terminal equivalent model, where $m_1$ is the turn ratio of an ideal transformer, $R_{SC}$ is the internal resistance called the SC resistance, and $R_L$ is the output load. In the SC dc/dc converter, it is known that the four-terminal equivalent model shown in Figure 3 can be obtained under the following conditions: 1) all of circuit components have negligibly small parasitic elements and 2) the time constant of the converter is much larger than a period of clock pulses. To deal with the proposed ac/dc converter as a dc/dc converter, we assume an ac input as a staircase ac waveform. In other words, the maximum power efficiency and maximum output voltage are derived theoretically in this analysis.

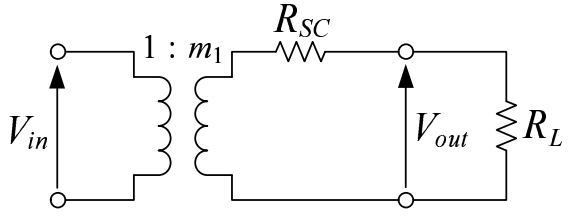


FIGURE 3. Four-terminal equivalent model

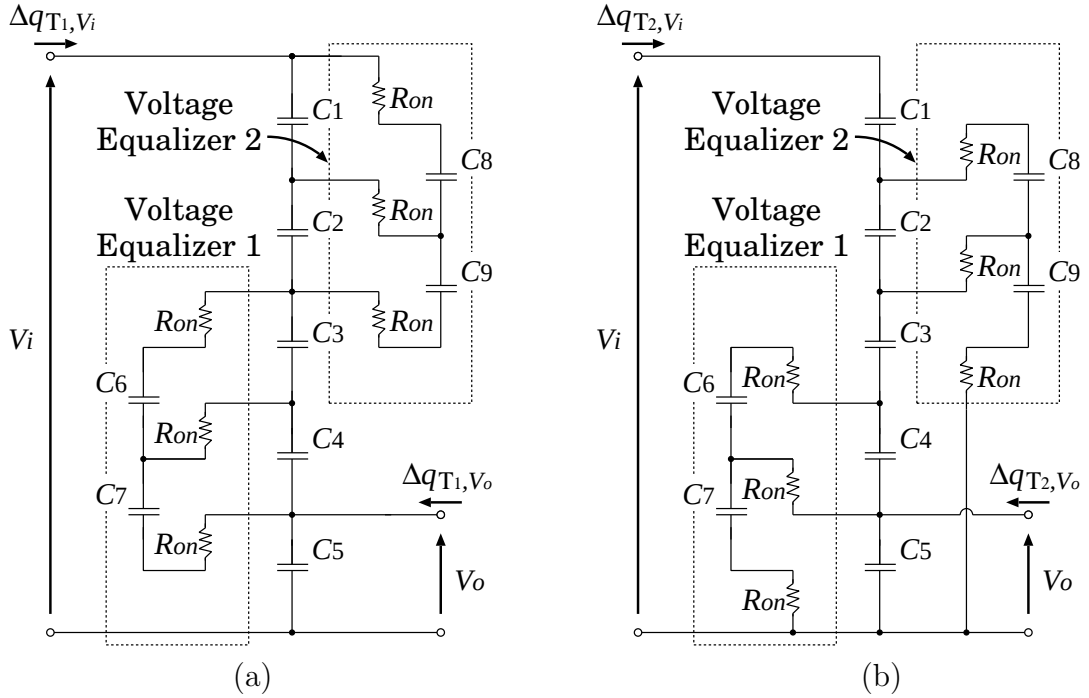


FIGURE 4. Instantaneous equivalent circuits of the converter blocks; (a) State-$T_1$ and (b) State-$T_2$

In a steady state, the instantaneous equivalent circuits of the proposed converter are illustrated in Figure 4. As Figure 4 shows, the proposed converter has two states in $T_i$ $(i = 1, 2)$: State-$T_1$ and State-$T_2$. By using these instantaneous equivalent circuits, we obtain the parameters $m_1$ and $R_{SC}$ in Figure 3. At the start and end of the cycle $T$ in a steady state, the electric charge in $C_k$ $(k = 1, \ldots, 9)$ has to be the same. Therefore, the following equations are satisfied concerning the differential value of the electric charge in $C_k$:

$$\begin{aligned} &\Delta q^k_{T_1} + \Delta q^k_{T_2} = 0, \\ \text{where} \qquad &T = T_1 + T_2 \qquad \text{and} \qquad T_1 = T_2 = \frac{T}{2}. \end{aligned} \tag{3}$$

In (3), $\Delta q^k_{T_i}$ denotes the electric charge of the $k$-th capacitor in State-$T_i$. From Figure 4(a), the relations between the differential values of electric charges in State-$T_1$ are given by

$$\begin{aligned} &\Delta q_{T_1,V_i} = \Delta q^1_{T_1} + \Delta q^8_{T_1}, \\ &\Delta q_{T_1,V_o} = -\Delta q^4_{T_1} + \Delta q^5_{T_1} - \Delta q^7_{T_1}, \\ &\Delta q^4_{T_1} = \Delta q^3_{T_1} + \Delta q^6_{T_1} - \Delta q^7_{T_1}, \\ &\Delta q^3_{T_1} = \Delta q^2_{T_1} - \Delta q^6_{T_1} + \Delta q^9_{T_1}, \\ \text{and} \qquad &\Delta q^2_{T_1} = \Delta q^1_{T_1} + \Delta q^8_{T_1} - \Delta q^9_{T_1}, \end{aligned} \tag{4}$$

where $\Delta q_{T_1,V_i}$ and $\Delta q_{T_1,V_o}$ are the differential values of electric charges in $V_i$ and $V_o$, respectively. On the other hand, from Figure 4(b), the relations between the differential values of electric charges in State-$T_2$ are given by

$$\begin{aligned} &\Delta q_{T_2,V_i} = \Delta q^1_{T_2}, \\ &\Delta q_{T_2,V_o} = -\Delta q^4_{T_2} + \Delta q^5_{T_2} - \Delta q^6_{T_2} + \Delta q^7_{T_2}, \end{aligned}$$

$$\begin{aligned} \Delta q_{T_2}^4 &= \Delta q_{T_2}^3 - \Delta q_{T_2}^6, \\ \Delta q_{T_2}^3 &= \Delta q_{T_2}^2 + \Delta q_{T_2}^8 - \Delta q_{T_2}^9, \\ \text{and} \qquad \Delta q_{T_2}^2 &= \Delta q_{T_2}^1 - \Delta q_{T_2}^8, \end{aligned} \tag{5}$$

where $\Delta q_{T_2,V_i}$ and $\Delta q_{T_2,V_o}$ are the differential values of electric charges in $V_i$ and $V_o$, respectively. Here, the turn ratio of an ideal transformer in Figure 3, $m_1$, can be obtained by the relation between the input current and the output current. By combining (3)-(5), the average input current and the average output current can be expressed as

$$\overline{I_i} = \frac{1}{T}\left(\sum_{i=1}^{2} \Delta q_{T_i,V_i}\right) = \frac{\Delta q_{V_i}}{T} \quad \text{and} \quad \overline{I_o} = \frac{1}{T}\left(\sum_{i=1}^{2} \Delta q_{T_i,V_o}\right) = \frac{\Delta q_{V_o}}{T}, \tag{6}$$

where $\Delta q_{V_i}$ and $\Delta q_{V_o}$ are electric charges in the input/output terminals. By solving the algebraic equations of (3)-(6), we have the relation between the input and output currents as follows:

$$\overline{I_i} = -\frac{1}{9}\overline{I_o}, \quad \text{where} \quad \Delta q_{V_i} = -\frac{1}{9}\Delta q_{V_o}. \tag{7}$$

From (7), the parameter $m_1$ of Figure 3 is obtained as

$$m_1 = \frac{1}{9}. \tag{8}$$

Next, the derivation of the parameter $R_{SC}$ is described by considering the consumed energy of Figure 4. The consumed energy of Figure 4(a), $W_{T_1}$, can be expressed by

$$\begin{aligned} W_{T_1} = {} & \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^8\right)^2 + \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^8 - \Delta q_{T_1}^9\right)^2 + \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^9\right)^2 \\ & + \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^6\right)^2 + \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^6 - \Delta q_{T_1}^7\right)^2 + \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^7\right)^2. \end{aligned} \tag{9}$$

By substituting (3)-(5) into (9), the consumed energy in State-$T_1$ can be rewritten as

$$W_{T_1} = \frac{20R_{on}}{27T_1}(\Delta q_{V_o})^2. \tag{10}$$

On the other hand, the consumed energy of Figure 4(b), $W_{T_2}$, can be expressed by

$$\begin{aligned} W_{T_2} = {} & \frac{R_{on}}{T_2}(\Delta q_{T_2}^8)^2 + \frac{R_{on}}{T_2}(\Delta q_{T_2}^8 - \Delta q_{T_2}^9)^2 + \frac{R_{on}}{T_2}(\Delta q_{T_2}^9)^2 \\ & + \frac{R_{on}}{T_2}(\Delta q_{T_2}^6)^2 + \frac{R_{on}}{T_2}(\Delta q_{T_2}^6 - \Delta q_{T_2}^7)^2 + \frac{R_{on}}{T_2}(\Delta q_{T_2}^7)^2. \end{aligned} \tag{11}$$

By substituting (3)-(5) into (11), the consumed energy in State-$T_2$ can be rewritten as

$$W_{T_2} = \frac{20R_{on}}{27T_2}(\Delta q_{V_o})^2. \tag{12}$$

By combining (10) and (12), we have the total consumed energy as follows:

$$W_T = \sum_{i=1}^{2} W_{T_i} = \frac{80R_{on}}{27T}(\Delta q_{V_o})^2. \tag{13}$$

In the four-terminal equivalent model of Figure 3, the consumed energy is defined by

$$W_T := \left(\frac{\Delta q_{V_o}}{T}\right)^2 \cdot R_{SC} \cdot T, \tag{14}$$

because energy is consumed only by the SC resistance $R_{SC}$. By comparing (13) with (14), the parameter $R_{SC}$ is obtained as

$$R_{SC} = \frac{80R_{on}}{27}. \tag{15}$$

Finally, we can have the four-terminal equivalent model by combining (8) and (15). In other words, the equivalent model of the proposed converter can be expressed by the following K-matrix:

$$\begin{bmatrix} \overline{V_i} \\ \overline{I_i} \end{bmatrix} = \begin{bmatrix} 9 & 0 \\ 0 & 1/9 \end{bmatrix} \begin{bmatrix} 1 & 80R_{on}/27 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_o} \\ -\overline{I_o} \end{bmatrix}. \tag{16}$$

From (16), the maximum power efficiency $\eta$ and the maximum output voltage $V_{out}$ can be estimated as follows:

$$\eta = \frac{R_L}{R_L + R_{SC}} = \frac{R_L}{R_L + 80R_{on}/27} \tag{17}$$

$$\text{and} \qquad V_{out} = \left(\frac{R_L}{R_L + R_{SC}}\right) \times \frac{V_i}{9} = \left(\frac{R_L}{R_L + 80R_{on}/27}\right) \times \frac{V_i}{9}. \tag{18}$$

As you can see from (17) and (18), $R_{SC}$ is one of the most important factors to achieve high power efficiency. The smaller $R_{SC}$ leads to the higher power efficiency.

The comparison result of the SC resistance between the proposed converter and the conventional converters reported in [2, 11, 12] is drawn in Table 1. As Table 1 shows, the SC resistance of the proposed converter is the same as that of the conventional converter reported in [12]. In the conversion ratio of 1/9, the proposed converter can achieve the highest power efficiency among them, because the SC resistance of the proposed converter is smaller than that of the conventional converters.

The comparison result of the number of circuit components between the proposed converter and the conventional converters reported in [2, 11, 12] is drawn in Table 2. As Tables 1 and 2 show, the number of circuit components for the conventional converter [11] is the smallest, though $R_{SC}$ of the conventional converter reported in [11] is the largest. However, the difference between the proposed converter and the conventional converter reported in [11] is only one capacitor.

Table 1. Comparison of the internal resistances

| | $R_{SC}$ | Step-down ratio |
|---|---|---|
| Proposed converter | $80R_{on}/27$ | 1/9 |
| Conventional converter [2] | $280R_{on}/81$ | 1/9 |
| Conventional converter [11] | $40R_{on}/9$ | 1/9 |
| Conventional converter [12] | $80R_{on}/27$ | 1/9 |

Table 2. Comparison of the number of circuit components

| | Power switch | Capacitor | Diode | Total |
|---|---|---|---|---|
| Proposed converter | 12 | 10 | 4 | 26 |
| Conventional converter [2] | 28 | 10 | 4 | 42 |
| Conventional converter [11] | 12 | 9 | 4 | 25 |
| Conventional converter [12] | 12 | 11 | 4 | 27 |

4. **Simulation.** In this section, the characteristics of the proposed converter are investigated by using the SPICE simulator. In the SPICE simulations, the proposed ac/dc converter was compared with the conventional converters [2, 11, 12] realizing a fixed conversion ratio, because the proposed ac/dc converter provides the fixed conversion ratios. Furthermore, to compare the proposed converter with the state-of-the-art converters [11, 12], the conversion ratio was set to 1/9, because the series-connected ac/dc converters [11, 12] cannot offer the conversion ratios of the prime number such as 1/7×. Of course, unlike the series-connected ac/dc converters [11, 12], the proposed converter can provide other conversion ratios by combining voltage equalizers. To show the flexibility of conversion ratio of the proposed converter, an example of the proposed converter realizing the 1/7× step-down conversion will be described in Appendix.

In SPICE simulations, output voltages and power efficiency were demonstrated under conditions that $V_{in} = 100\text{V@50Hz}$, $T = 1\mu\text{s}$, $R_{on} = 0.1\Omega$, $C_0 = 99\mu\text{F}$ and $C_{1,k} = C_{2,k} = 33\mu\text{F}$. Figure 5 demonstrates the simulated output voltage of the proposed converter as a function of time. As you can see from Figure 5, the proposed converter can offer the 1/9× stepped-down DC voltage to the output load $R_L$ (= 100Ω). Of course, the proposed converter can offer various types of output voltages by combining voltage equalizers. The comparison of output voltages between the proposed converter and the conventional converters [2, 11, 12] is shown in Figure 6. As Figure 6 shows, the output voltage of the proposed converter is higher than that of the conventional converters [2, 11]. Furthermore, the number of circuit components for the proposed converter is smaller than that of the conventional converter [12] (see Table 2), though the output voltage of the proposed converter is almost the same as that of the conventional converter [12]. The simulated result of Figure 6 agrees well with the theoretical result described in Section 3. As (18) shows, the voltage drop of the simulated voltage depends on the SC resistance $R_{SC}$.

Figure 7 demonstrates the comparison of output ripples between the proposed converter and the conventional converters [2, 11, 12]. As Figure 7 shows, the proposed converter can achieve smaller ripple noise than the conventional converters [2, 11]. However, the output ripple of the proposed converter is larger than that of the conventional converter [12], because the synthetic capacity of main capacitors for the proposed converter is smaller than that for the conventional converter [12].

Figure 8 shows the simulated power efficiency as a function of the output power. As you can see from Figure 8, the power efficiency of the proposed converter is higher than

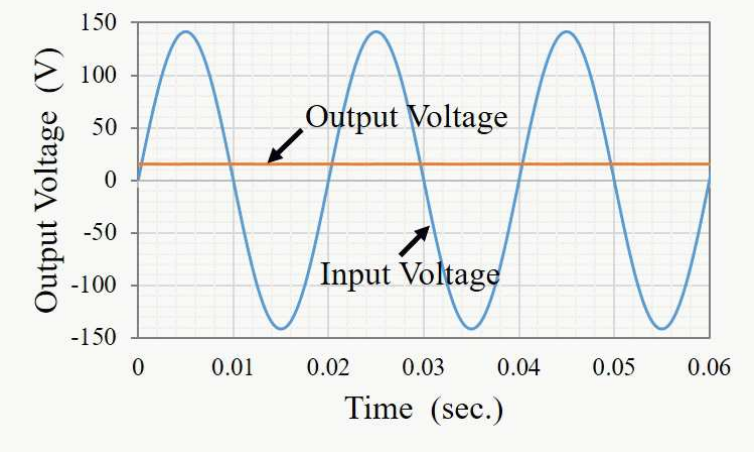


FIGURE 5. Simulated output voltage of the proposed converter when the output load is 100Ω

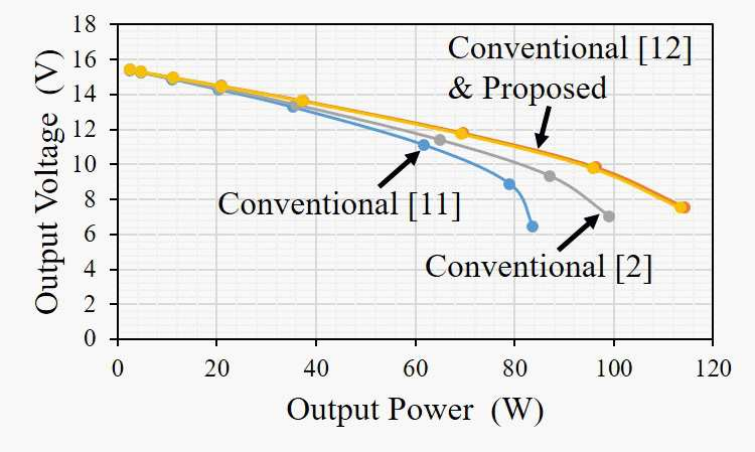


FIGURE 6. Simulated output voltages as a function of the output power

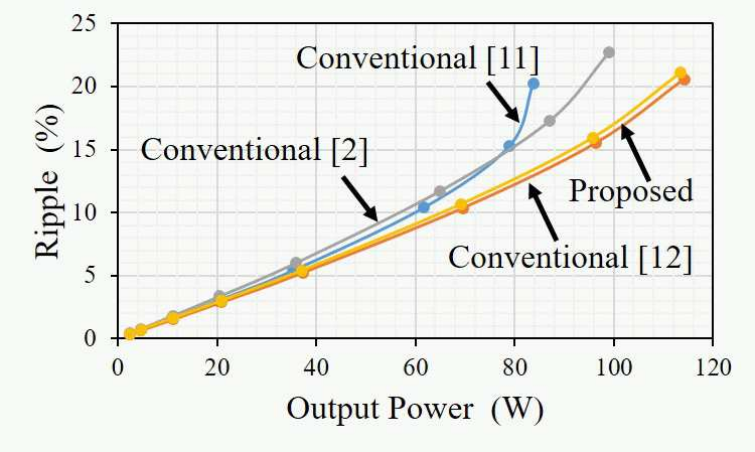


FIGURE 7. Simulated ripples as a function of the output power

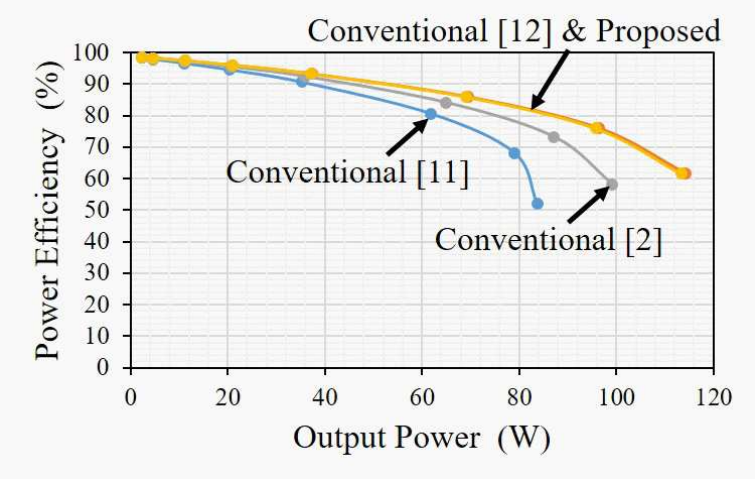


FIGURE 8. Simulated power efficiency as a function of the output power

that of the conventional converters [2, 11]. On the other hand, the power efficiency of the proposed converter is almost the same as that of the conventional converter [12].

TABLE 3. Summary of comparison results

| | Size | Efficiency | Voltage drop | Ripple |
|---|---|---|---|---|
| Proposed converter | 2 | 1 | 1 | 2 |
| Conventional converter [2] | 4 | 3 | 3 | 4 |
| Conventional converter [11] | 1 | 4 | 4 | 3 |
| Conventional converter [12] | 3 | 1 | 1 | 1 |

1: Best $\longleftrightarrow$ 4: Worst.

The proposed converter and the conventional converter [12] can achieve more than 90% efficiency when the output power is less than 50W.

Table 3 shows the summary of comparison results. Obviously, the proposed converter achieves a better performance than the conventional converters [2, 11]. Compared with the conventional converter [12], the performance of the proposed converter is almost the same. However, the proposed converter can realize various types of conversion ratios by combining voltage equalizers.

5. **Experiments.** To confirm the validity of circuit design, an example of the experimental circuit of the proposed converter was implemented on a breadboard. The experimental circuit of the proposed converter is demonstrated in Figure 9. The experimental circuit of Figure 9 was built on a breadboard by using commercially available circuit components shown in Table 4, where a small transformer was connected between the commercial power source and the experimental circuit in order to isolate the power source from the output load. In the experimental circuit of Figure 9, the photo MOS relay was used in substitution for MOS switch. To drive the photo MOS relays, Darlington transistor arrays were connected between the photo MOS relays and the micro-controller that generates clock pulses.

Figure 10 demonstrates the measured output voltage of the experimental circuit shown in Figure 9. In Figure 10, the input voltage was set to $V_{in}$ = 141V@60Hz, the period of clock pulses was set to $T = 100\mu$s, and the turn ratio of the transformer between the primary side and the secondary side was set to 1 : 1. However, due to component fluctuations in the transformer, the practical turn ratio was 1 : 1.13. For this reason,

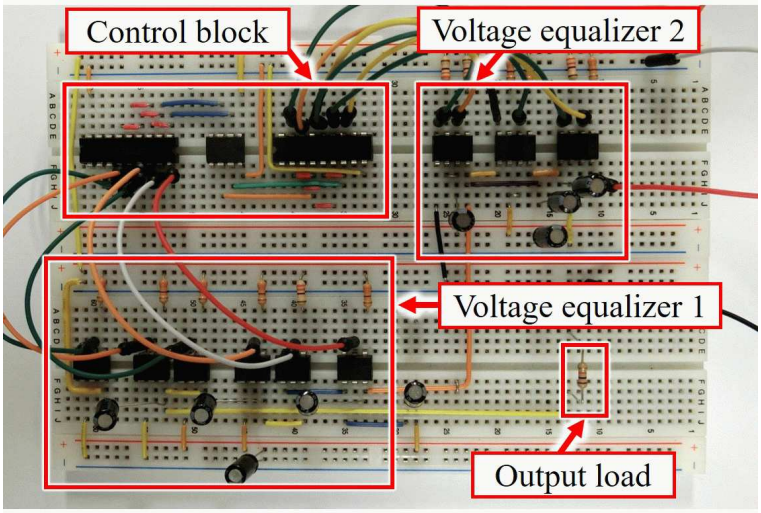


FIGURE 9. Experimental circuit of the proposed converter

TABLE 4. Circuit components of the experimental converters

| Parts | Components | Models |
|---|---|---|
| Full bridge circuit | Diode switch | 1N4007 |
| | Capacitor | 165$\mu$F |
| Control block | Micro controller | PIC12F1822 |
| | Darlington driver IC | TDG2083APG |
| | Current control resistance | 330$\Omega$ |
| Voltage equalizer | Power switch | AQV212 |
| | Capacitor | 33$\mu$F |
| Output load | Resistance | 10k$\Omega$ |

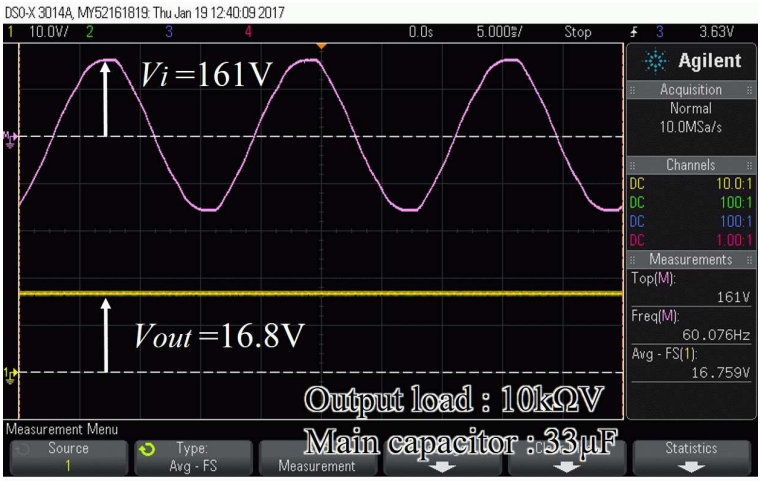


FIGURE 10. Measured output voltage of the experimental circuit

in Figure 10, the measured input voltage was about 161V ($\simeq$ 141V $\times$ 1.13). In other words, the input voltage of the experimental circuit is 113V@60Hz. As Figure 10 shows, the measured output voltage of the proposed converter is about 16.8V when the output load is 10k$\Omega$. Figure 11 shows the measured voltages of the main capacitors $C_1 \sim C_5$. As Figure 11 shows, the voltage ratio of main capacitors is $C_1 : C_2 : C_3 : C_4 : C_5 = 1 : 1 : 1 : 3 : 3$. Therefore, about 1/9$\times$ stepped-down voltage is offered by the experimental circuit. The feasibility of the proposed converter can be confirmed by the experimental results of Figures 10 and 11.

6. **Conclusions.** For small power applications, a nesting-type SC ac/dc converter using voltage equalizers has been proposed in this paper. By nesting the voltage equalizers in the proposed converter, a part of the capacitor voltage of a voltage equalizer is converted by other voltage equalizers. By the nesting conversion, the conversion ratio of the proposed converter is expressed as a reverse value of the total sum of main capacitors' voltage ratios.

Concerning the 1/9$\times$ step-down SC ac/dc converter, we investigated the advantages of the proposed converter by theoretical analysis, SPICE simulations, and experiments. In the theoretical analysis, a four-terminal equivalent model of the proposed converter was derived theoretically. From the equivalent circuit, we obtained the maximum power efficiency and the maximum output voltage, theoretically. The theoretical results revealed that the SC resistance of the proposed converter is smaller than conventional converters. Hence, the proposed converter can achieve higher power efficiency and smaller voltage

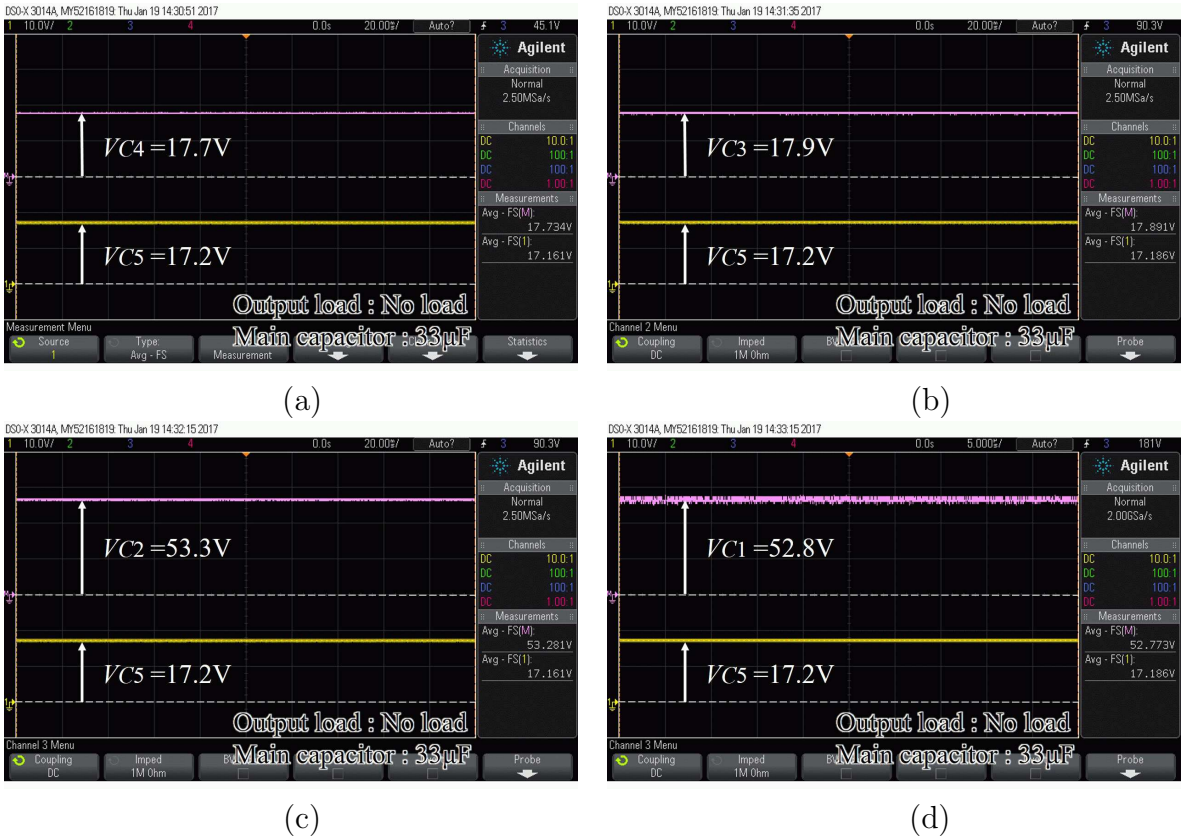


FIGURE 11. Measured voltage of capacitors; (a) $C_5$ vs. $C_4$, (b) $C_5$ vs. $C_3$, (c) $C_5$ vs. $C_2$, and (a) $C_5$ vs. $C_1$

drop than conventional converters. However, the SC resistance of the proposed converter was the same as that of the conventional converter with double conversion topology.

To confirm the validity of the theoretical analysis, SPICE simulations were conducted concerning the proposed converter and conventional converters. The simulation results agreed well with the theoretical results. In the SPICE simulations, the proposed converter achieved more than 90% efficiency and less than 7% output ripple when the output power was less than 50W. Furthermore, the proposed converter can reduce one capacitor from the conventional converter with double conversion topology, though the power efficiency and the voltage drop of the proposed converter were almost the same as that of the conventional converter with double conversion topology.

In the experiments, we verified the feasibility of the proposed converter by using the experimental circuit implemented on a breadboard. When the output load was 10kΩ, the experimental circuit generated about 17V DC output by converting a 113V@60Hz AC input. The experimental circuit can provide the 1/9× stepped-down voltage, because the voltage ratio of main capacitors was demonstrated as $C_1 : C_2 : C_3 : C_4 : C_5 = 1 : 1 : 1 : 3 : 3$. From these results, the feasibility and effectiveness of the proposed converter were confirmed.

The hybrid IC implementation and its experimental analysis are left to a future study. In this work, the proposed converter was not implemented in a hybrid IC form. Therefore, the practical characteristics of the proposed converter including parasitic losses are not clear. In the future study, we are going to conduct the experiments concerning the implemented converter.

## REFERENCES


[1] I. Oota, F. Ueno, T. Inoue and H. B. Lian, Realization and analysis of new switched-capacitor AC-DC converters, *T. IEICE Trans.*, vol.E72, no.12, pp.1292-1298, 1989.

[2] I. Oota, F. Ueno, T. Inoue and H. B. Lian, Realization of a switched-capacitor AC-DC converter with a low output-voltage ripple and its design, *T. IEICE Trans.*, vol.E73, no.9, pp.1434-1441, 1990.

[3] I. Oota, I. Harada, T. Inoue and F. Ueno, High efficiency control method of switched-capacitor AC-DC converter, *T. IEICE Trans.*, vol.J76, no.6, pp.422-431, 1993.

[4] K. Eguchi, H. Zhu, I. Oota, S. Terada and F. Ueno, A novel control method of a switched-capacitor AC-DC converter for small power applications, *Proc. of the 4th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology*, pp.317-320, 2007.

[5] I. Oota, N. Hara and F. Ueno, An AC-DC converter using a differential switched-capacitor transformer, *Proc. of the 1998 IEEE Power Electronics Specialists Conference*, vol.2, pp.763-769, 1998.

[6] N. Hara, I. Oota, F. Ueno and I. Harada, A programmable ring type switched-capacitor AC-DC converter, *Proc. of the 1999 International Symposium on Nonlinear Theory and Its Applications*, vol.1, pp.159-162, 1999.

[7] S. Terada, I. Oota, K. Eguchi and F. Ueno, A ring type switched-capacitor (SC) programmable converter with DC or AC input/DC or AC output, *Proc. of the 47th IEEE International Midwest Symposium on Circuits and Systems*, pp.29-32, 2004.

[8] S. Terada, I. Oota, K. Eguchi and F. Ueno, Separate type switched-capacitor (SC) AC-DC converter, *Proc. of the 2006 IEEE International Symposium on Circuits and Systems*, pp.5055-5058, 2006.

[9] K. Eguchi, I. Oota, S. Terada and T. Inoue, A design method of switched-capacitor power converters by employing a ring-type power converter, *International Journal of Innovative Computing, Information and Control*, vol.5, no.10(A), pp.2927-2938, 2009.

[10] S. Hirakawa, S. Terada, K. Eguchi and I. Oota, AC-DC converter using digital-selecting type switched-capacitor, *Proc. of the 25th International Technical Conference on Circuits/Systems, Computers and Communications*, pp.474-477, 2010.

[11] K. Abe, I. Oota, W. L. Do, S. Kittipanyangam and K. Eguchi, Design of a step-down switched-capacitor AC/DC converter with series-connected converter blocks, *ICIC Express Letters*, vol.10, no.8, pp.2045-2050, 2016.

[12] K. Abe, K. Smerpitak, S. Pongswatd, I. Oota and K. Eguchi, A step-down switched-capacitor AC-DC converter with double conversion topology, *International Journal of Innovative Computing, Information and Control*, vol.13, no.1, pp.319-330, 2017.

[13] R. L. Andersen, T. B. Lazzarin and I. Barbi, A 1-kW step-up/step-down switched-capacitor AC-AC converter, *IEEE Trans. Power Electronics*, vol.28, no.7, pp.3329-3340, 2013.

[14] T. B. Lazzarin, R. L. Andersen and I. Barbi, A switched-capacitor three-phase AC-AC converter, *IEEE Trans. Industrial Electronics*, vol.62, no.2, pp.735-745, 2015.

[15] K. Eguchi, I. Oota, S. Terada and H. Zhu, Synthesis and analysis of a switched-capacitor-based battery equalizer using level-shift circuits, *International Journal of Intelligent Engineering and Systems*, vol.5, no.4, pp.1-9, 2012.

[16] K. Eguchi, P. Julsereewong, A. Julsereewong, K. Fujimoto and H. Sasaki, A Dickson-type adder/subtractor DC-DC converter realizing step-up/step-down conversion, *International Journal of Innovative Computing, Information and Control*, vol.9, no.1, pp.123-138, 2013.

[17] K. Eguchi, I. Oota, S. Terada and H. Zhu, A hybrid-input negative ring-type converter using clean energy power supplies, *International Journal of Intelligent Engineering and Systems*, vol.5, no.3, pp.1-10, 2012.

[18] K. Eguchi, T. Sugimura, S. Pongswatd, K. Tirasesth and H. Sasaki, Design of a multiple-input parallel SC DC-DC converter and its efficiency estimation method, *ICIC Express Letters*, vol.3, no.3(A), pp.531-536, 2009.

## Appendix.

**Circuit configuration.** To demonstrate the flexibility of the proposed converter, the proposed converter realizing the 1/7× step-down conversion is discussed in this section. Figure 12 illustrates the circuit configuration of the proposed converter realizing the 1/7× step-down conversion. The operation principle of Figure 12 is as follows. In the voltage equalizer 1, the flying capacitors $C_6$ and $C_7$ are connected to $C_3$ and $C_4$ in State-$T_1$. In this timing, the voltage of $C_3$ becomes the same as that of $C_4$. Next, $C_6$ and $C_7$ are connected to $C_4$ and $C_5$ in State-$T_2$. In this timing, the voltage of $C_4$ becomes the same as that of $C_5$. Therefore, the voltage ratio of capacitors $C_3$, $C_4$, and $C_5$ becomes $1:1:1$. Similarly, in the voltage equalizer 2, the flying capacitors $C_8$ and $C_9$ are connected to $C_1$ and $C_2$ in State-$T_1$. In this timing, the voltage of $C_1$ becomes the same as that of $C_2$. Next, in State-$T_2$, the flying capacitors $C_8$ and $C_9$ are connected to the capacitors $C_2$ and the series-connected capacitors $C_3$ and $C_4$, respectively. In this timing, the voltage of $C_2$ becomes the same as that of the series-connected capacitors $C_3$ and $C_4$. By repeating these processes, the voltage ratio of capacitors $C_1$, $C_2$, $C_3$, $C_4$, and $C_5$ becomes $2:2:1:1:1$. Therefore, the output voltage $V_o$ becomes

$$V_o = \frac{V_{C5}}{\sum_{i=k}^{5} V_{Ck}} \times V_i = \frac{V_{C5}}{V_{C5}(2+2+1+1+1)} \times V_i = \frac{1}{7} V_i. \tag{19}$$

As (19) shows, the proposed converter can offer flexible conversion ratios, though the conventional converter [12] cannot offer the conversion ratios of the prime number.

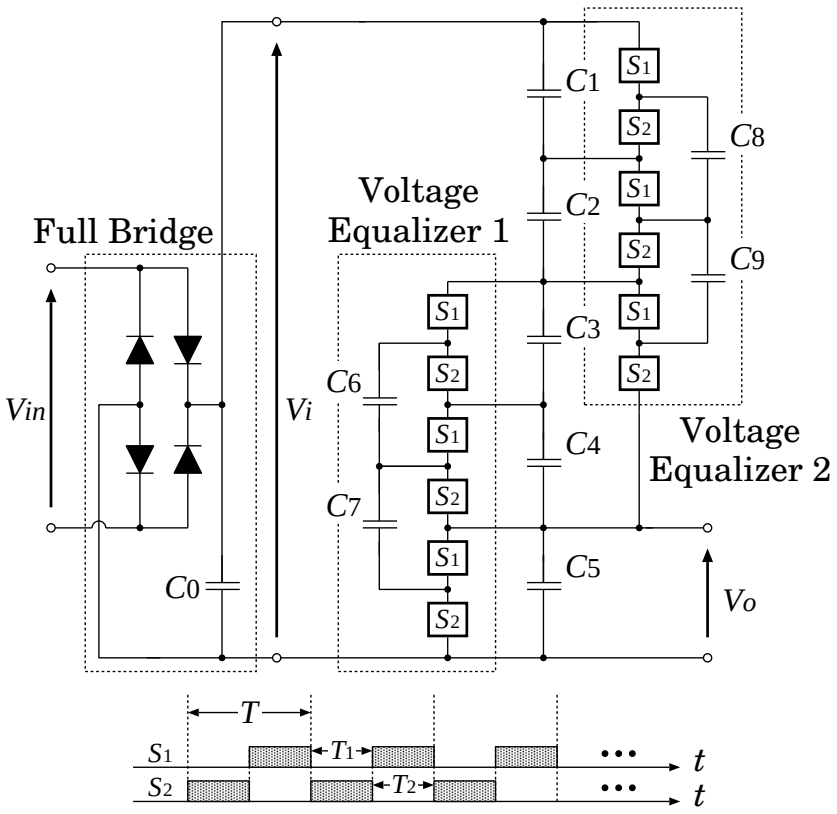


FIGURE 12. Proposed SC ac/dc converter realizing the 1/7× step-down conversion

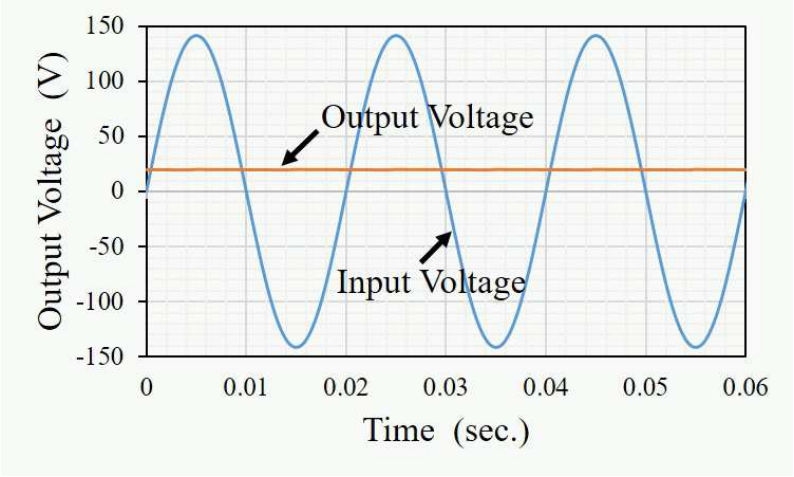


FIGURE 13. Simulated output voltage when the output load is 100Ω

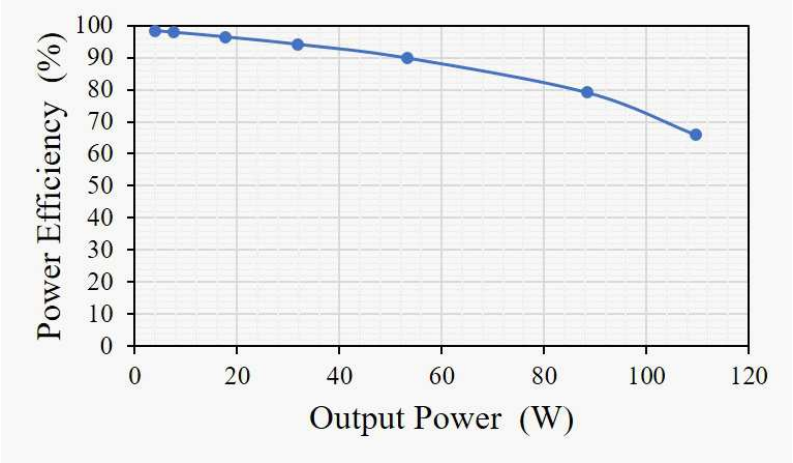


FIGURE 14. Simulated power efficiency as a function of the output power

**Simulation.** To validate the circuit design of Figure 12, we performed the SPICE simulation. Concerning the proposed converter realizing the 1/7× step-down conversion, the output voltage and power efficiency were demonstrated under conditions that $V_{in}$ = 100V@50Hz, $T = 1\mu$s, $R_{on} = 0.1\Omega$, $C_0 = 99\mu$F and $C_{1,k} = C_{2,k} = 33\mu$F. Figure 13 demonstrates the simulated output voltage of the proposed converter as a function of time. As Figure 13 shows, the proposed converter can offer the 1/7× stepped-down DC voltage to the output load $R_L$ (= 100Ω). Figure 14 shows the simulated power efficiency as a function of the output power. From Figure 14, the proposed converter can achieve more than 90% efficiency when the output power is less than 50W. Of course, the power efficiency depends on the on-resistance of switches and the capacity of $C_0$.