

STABILITY AND INERTIA RESPONSE IMPROVEMENT OF BOOST CONVERTERS INTERLACED WITH CONSTANT POWER LOADS

MEHRAN JAMI¹, QOBAD SHAFIEE¹, KEI EGUCHI² AND HASSAN BEVRANI¹

¹Department of Electrical Engineering
University of Kurdistan

Pasdaran St., Sanandaj, Kurdistan 66177-15175, Iran
m.jami@eng.uok.ac.ir; {q.shafiee; bevrani}@uok.ac.ir

²Department of Information Electronics
Fukuoka Institute of Technology

3-30-1 Wajirohigashi, Higashi-ku, Fukuoka 811-0295, Japan
eguti@fit.ac.jp

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ABSTRACT. *In dc microgrids, the distributed sources and loads with different electrical characteristics are typically interconnected to the main bus through power electronic converters. The existence of interfaced converters creates two major problems: 1) the load-side converters and their associated loads, usually considered as constant power loads (CPLs), introduce destabilizing effects into the system; 2) the source-side converters do not possess any inertia or damping properties but reduce the overall inertia of the system. To overcome the stability problems caused by CPLs and low inertia, this paper proposes an active damping strategy based on a linear feedback. The proposed strategy measures the inductor current implemented in source-side boost converter in order to enhance the damping of the dc microgrids with CPLs. The control input-to-output voltage transfer function of a boost converter loaded with a CPL is inherently nonlinear, unstable and a non-minimum phase system that makes its control very difficult. In addition, the synthetic inertia of dc bus is enhanced by adding the virtual inertia control to the inner current control loop that is fast enough to emulate inertia and damping coefficient concept. In order to study the stability of dc MG with CPLs, a comprehensive small-signal model is derived and then, an acceptable range of inertia response parameters is determined by using the system's root locus analysis. Performance of the proposed control structure is demonstrated through numerical simulations.*

Keywords: Boost converter, Constant power load, Dc microgrid, Dynamic response, Virtual capacitance, Virtual damping, Virtual inertia

1. **Introduction.** Compared with the traditional ac microgrid (MG), a dc MG has several advantages, such as, higher efficiency with less power electronic devices, and simple control system design with no frequency and reactive power related issues [1-3]. Furthermore, dc MGs are better suited for combination of energy sources (e.g., PV system, battery, super capacitor) and loads (e.g., solid-state LED lighting, dc ventilation, dc data center, EV charger) because almost all of them are inherently dc [4,5]. These systems are being widely founded in more electric aircraft, naval ships, data centers, remote areas, banks and hospitals [3].

Power electronic converters play a key role in dc MGs where voltage, current or power regulation is required. To interconnect energy sources and loads with different electrical characteristics, power electronic converters are included between sources, loads and main

dc bus. In a typical power grid, linear passive loads, such as induction motors and incandescent bulbs consume all the electric power. However, in a modern power grid, these loads are connected to the dc MG through fast-response load-side power electronic converters. These active loads include devices such as LED lighting and motor drive systems like inverter appliances, back-to-back converter configurations, and consumer electronics with unity power factor correction [6,7]. Similarly, distributed generations (DGs), such as solar photovoltaic, wind, and energy storage systems (ESSs), are usually connected to the dc MG through source-side power electronic converters [8]. Hence, dc MGs usually include cascade distributed power structures in which power electronic converters act as interfaces between system stages with different voltage levels [9,10]. A schematic diagram of a typical dc MG is presented in Figure 1. It consists of one or more power sources, a local dc bus, a main dc bus, and a variety of possible loads. Renewable energy source (RES) units [such as photovoltaic (PV) and wind turbine systems] are used to provide clean energy, while ESS unit is utilized to compensate power fluctuation between power generation and consumption. The wind turbine, the PV, the ESS are, respectively, connected to the local dc bus through a unidirectional ac/dc, a unidirectional dc/dc and a bidirectional dc/dc converter. The utilized hybrid energy resource provides an almost constant dc bus voltage for the source-side boost converter. The source-side boost converter regulates the main dc bus voltage, such as the one located between the main dc bus and the local dc bus. At the last stage, one of the loads in the system is a resistor load which is directly connected to the main dc bus. The other loads are a motor drive, data center, and a combination of a load-side converter tightly regulating its output voltage and an output resistor. These loads can be regarded as a CPL.

Despite the advantages of cascaded distributed dc-dc converters, there are two major disadvantages.

i) The reduction in system inertia and damping. The main reason for lack of inertia is due to the source-side power electronic converters that are usually installed to connect the DGs to the main dc bus. These converters do not possess any inertia or damping properties and will make an instability for the system [11].

ii) The loads are connected to the main dc bus through tightly regulated load-side converters. These load-side converters and their associated loads are considered as constant power loads (CPLs) which introduce destabilizing effects into the system [12,13].

The integration of large number of power electronic interfaced generators reduces the natural inertia and governor damping which are inherent features of a synchronous machine (SM) [14]. Hence, when system inertia and/or damping decrease, the rate of change of frequency (RoCoF) and frequency deviation are increased. As a result, rapid and severe changes occur in system frequency, even at a small disturbance and may lead to MG instability. To enhance the inertia issue caused by source-side converter interfaced, the virtual synchronous generator (VSG) concept has been recently presented to provide *virtual inertia* to the power grid and hence improving its stability properties [15]. Note that inertia in dc MGs is indicated by the stability of dc bus voltage instead of frequency [5].

Taking the idea from power system and ac MGs, the concept of VSG is recently adapted to dc microgrids [16-18]. In [16], VSG with dual droop control is proposed for a dc-ac converter between the ac grid and various distributed energy resources (DER) connected on the dc side. In [17], a method is proposed to increase dc MG inertia by the analogy of ac VSG. Increasing the inertia of photovoltaic system [14], wind-battery-based grid [8], full cell generations [18], through inertia emulation in grid connected dc MGs are presented in the literature. Although these methods enhance the inertia of dc MGs, they are only applicable in grid-connected mode of operation. Furthermore, when the DERs

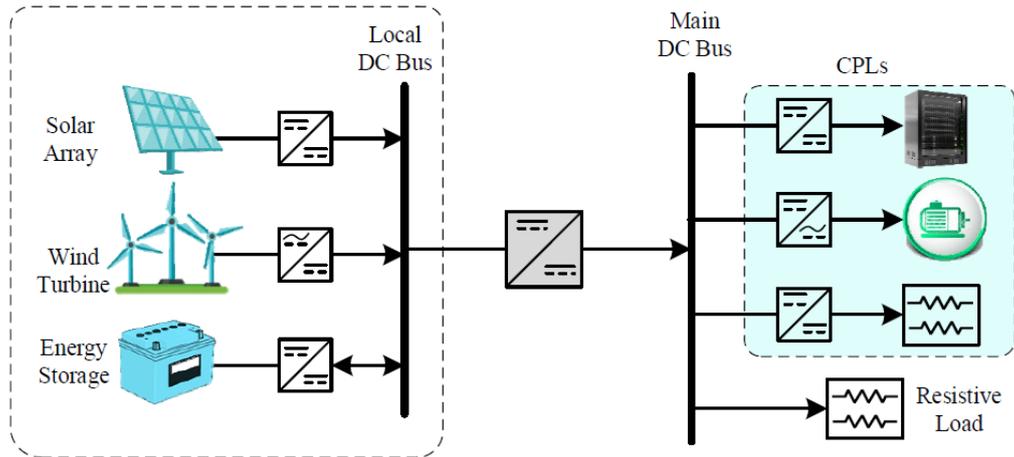


FIGURE 1. Structure of a typical dc MG

such as wind, full cell and solar are not available for power generation, the benefit of inertia emulation through DERs will not be available. In [19], a virtual inertia control (VIC) is designed to improve the dc bus voltage characteristic of the dc microgrid under both grid-connected and isolated modes. A novel coordinated control method with VI is implemented for reducing the bus voltage fluctuation in [20]. A VIC approach using a high pass filter is developed to control the voltage source converters (VSC) connected to a permanent magnet synchronous generator (PMSG) in a wind-battery based isolated dc microgrid [21], and using washout filter is developed [22] to control a dc-dc converter interfaced PV in a PV-battery based isolated dc microgrid. In [23], an adaptive droop control strategy is proposed to increase the inertia. A virtual dc machine concept is proposed in [24] to mimic the behavior of dc machines to control a bidirectional dc-dc converter connected with a storage device in a dc microgrid. In dc MGs, the inherent inertial support comes from the dc capacitors. Hence, large capacitors resist voltage fluctuations on the dc bus of an energy conversion/supply system. Due to the problems of electrolytic capacitors, such as bulky, expensive and short lifespan, larger dc capacitors are not acceptable [8]. In [5], a virtual capacitance control is proposed based on finite control set model predictive control to provide adaptive synthetic inertia support to the bus voltage. The aforementioned control strategies are inefficient in the presence of CPLs and the system may be unstable.

In multistage power grids, e.g., dc MGs, there are many converters loaded by other converters [25]. If the response of output regulating controller of load-side converter is fast enough, the load-side converter with the connected load can be considered as a CPL [26]. This means that when dc voltage changes, the controller regulates the load current to keep the absorbed power constant. For a CPL, the instantaneous value of impedance is positive and the incremental impedance is negative [7]. The negative incremental impedance makes the system poorly damped and can induce instable poles in the frequency domain which may destabilize the dc bus and consequently, the whole system [13]. In order to overcome this drawback, several methods based on hardware structure (passive damping) [28] or control modifications of converters (active damping) – on the source-side or on the load-side – have been proposed to alleviate the destabilizing effect of CPLs [27]. Strategies based on passive damping from load-side converters such as load shedding, addition of filters, resistive loads, and energy storage directly connected to the main dc bus are studied in [4]. Although passive damping can avoid instability by effectively converting a CPL

into a resistive load, this approach will increase the energy dissipation, size, weight, and cost; and will decrease the system efficiency [27-29].

Active damping, as an alternative, stabilizes the system from source-side converters instead of from CPL themselves [12]. Control-related methods seem to be a more practical solution without reducing system's efficiency. Due to the nonlinearity of converters and the negative-incremental impedance of CPLs, nonlinear control methods (e.g., sliding-mode control [10], loop-cancellation technique [25], geometric control, circular switching surfaces [30]) have been introduced to stabilize system. Comparing with linear control methods, nonlinear ones are limited in practice because of a high requirement for the hardware configuration, more complication and extra cost [26,27]. Consequently, linear control methods have been employed to enhance the stability of dc MGs with CPLs. In [27] and [29], active damping methods based on a super-capacitor and current mode control are presented to overcome the instability problems induced by the CPLs in the dc MG. In [12], a virtual resistance at the source-side converter of dc MGs is implemented. Authors in [31] introduce a virtual parallel resistive-inductive branch at the output of the source-side converters to overcome the disadvantage of virtual resistance i.e., poor voltage regulation. A virtual negative inductor [2] and virtual impedance [32] are constructed on the output of source-side converter. The constructed virtual negative inductor through the droop control method will counteract the large line inductance and virtual impedance modifies the output impedance of the source converter to match the input impedance of the cascaded CPL. However, these methods suffer from some disadvantages: 1) they are ineffective on providing inertia response, and 2) when step changes or random fluctuations occur from the intermittent power resources and load power, low frequency oscillation appears, which results in lower dc voltage quality.

Therefore, the existence of interfaced converters creates two major problems in dc MGs: 1) CPLs introduce destabilizing effects into the system, and 2) the reduction in system inertia and damping may lead to system instability. In order to overcome the CPL problems, nonlinear control methods [10,25,30] and linear control methods [2,12,27,31,32] have been employed. However, these control strategies do not improve the inertial response performance. Therefore, to solve low inertia issue, virtual inertia control has been presented [21,23,24]. In those works, the effect of CPLs, which is important for stability, has not been considered. As a result, active stabilization together with inertia control is an interesting solution to further improve dc bus voltage responses. However, up to now, only few research works have been reported, e.g., VIC of PV in an islanded dc MG with CPLs [22], and virtual capacitor for large-signal stabilization of a dc-Link supplying CPLs [33].

In this paper, an active damping based virtual inertia is introduced to stabilize isolated dc MGs loaded by CPLs. The proposed controller is implemented on the source-side converter of the system. The method of active damping is based on a linear feedback of inductor current to improve the stability margin of the interfaced converter and adds an inertia response loop to the output of the voltage controller. A comprehensive small-signal model is proposed for obtaining the optimal value of the inertia response parameter. The salient features of this work can be summarized as follows.

- The active damping strategy based on a linear feedback, measuring the inductor current is implemented in source-side boost converter in order to enhance the damping of isolated dc MGs with CPLs and guarantee the stable operation.
- Virtual inertia loop is implemented in inner current control loop. It proposes a derivative term which is fast enough to decrease rate of change of dc bus voltage (RoCoV) by using virtual capacitance. This emulates the virtual inertia concept.

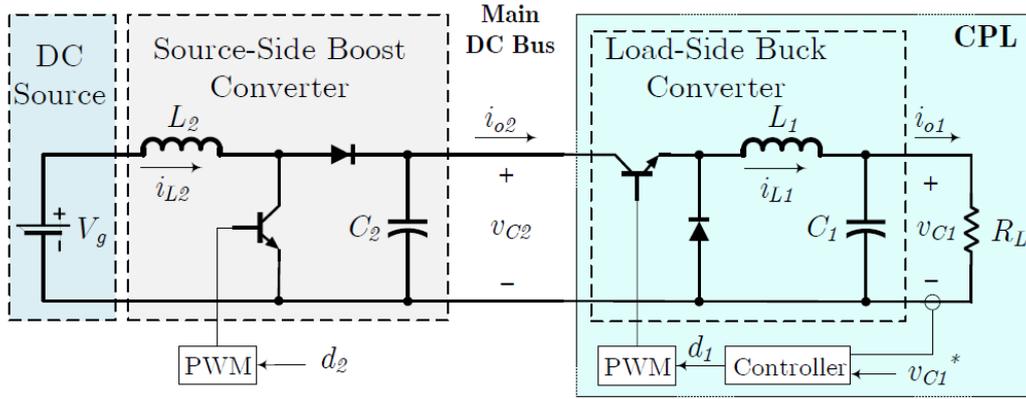
- The proposed proportional term in the virtual inertia loop increases damping of dc bus voltage by using virtual conductance that emulates damping coefficient concept.
- The small-signal stability is considered to study the system behavior under small disturbances or load perturbations at some steady-state operational points. The analysis is validated by using the eigenvalue analysis and time-domain simulation.

The remainder of this paper is organized as follows. Section 2 presents a multistage structure of dc MGs with CPLs and describes a comprehensive small-signal model of the described system. In Section 3, the proposed control strategy is introduced. The stability analysis of the system and parameters range selection in the presence of the proposed controller are presented in Section 4. Simulation studies are presented in Section 5. Section 6 concludes the paper.

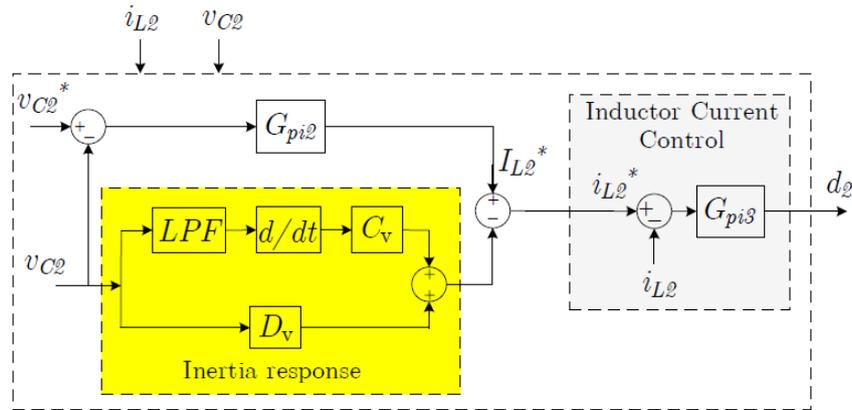
Nomenclature

C_1, C_2	Capacitor of load-side converter and source-side converter.
L_1, L_2	Inductor of load-side converter and source-side converter.
i_{L1}, i_{L2}	Inductor current of load-side converter and source-side converter.
i_{o1}, i_{o2}	Output current of load-side converter and source-side converter.
v_{C1}, v_{C2}	Capacitor voltage of load-side converter and source-side converter.
d_1, d_2	Duty cycle of load-side converter and source-side converter.
v_g	Local dc bus voltage.
R_L	Resistive load connected to load-side converter.
P_{CPL}	CPL power.
C_v	Virtual capacitance value.
D_v	Virtual damping value.
τ	Low pass filter time constant.
J	Moment of inertia.
D_p	Damping power coefficient.
ω	Rotor angular frequency.
ω_n	Nominal angular frequency.
P_{in}	Input mechanical power.
P_{out}	Output electrical power.
K_{p1}	Proportional coefficient of $G_{pi1}(s)$.
K_{p2}	Proportional coefficient of $G_{pi2}(s)$.
K_{p3}	Proportional coefficient of $G_{pi3}(s)$.
K_{i1}	Integral coefficient of $G_{pi1}(s)$.
K_{i2}	Integral coefficient of $G_{pi2}(s)$.
K_{i3}	Integral coefficient of $G_{pi3}(s)$.
$G_{pi1}(s)$	Voltage controller of load side converter.
$G_{pi2}(s)$	Voltage controller of source side converter.
$G_{pi3}(s)$	Current controller of source side converter.
$G_{LPF}(s)$	Low pass filter.
$G_{id}(s)$	Control input-to-inductor current transfer function.
$G_{vd}(s)$	Control input-to-output voltage transfer function.
$Z_{in-CL}(s)$	Closed-loop CPL impedance.
$Z_{IN-CL}(s)$	Closed-loop CPL resistance.
λ_i	Eigenvalues.
$(.)^*$	Nominal setpoint of the variable.
S	Steady-state represented by upper case letter.
\hat{s}	Small signal represented by lower case with hat.
s	Signal represented by lower case letter.

2. Modeling of Dc MGs with CPLs. Figure 2(a) shows a simplified dc distribution system. To simplify the model, the DGs and ESSs are replaced by an equivalent dc voltage source. Due to the rated voltage of each bus, different types of interface converters are selected. The main dc bus ($v_{C2} = 100$ V) is supplied by dc source ($V_g = 48$ V) through a source-side boost converter. For the load-side converter, a buck converter is selected that transforms the main dc bus voltage ($v_{C2} = 100$ V) to resistive load ($v_{C1} = 50$ V). Without losing generality, the internal resistance of the inductor, parasitic resistance and transmission line are neglected to simplify the calculations. Moreover, the interfaced CPL is modeled in detail. Here, subtitle “1” is used for CPL buck converter, and subtitle “2” is used for boost converter between dc source and CPL.



(a)



(b)

FIGURE 2. Simplified typical dc distribution system: (a) detailed power conversion circuit, (b) proposed control method for the source-side boost converter with virtual response and inductor current loop

2.1. Comprehensive small-signal model of the CPL. Let us assume that conventional proportional-integral (PI) controller is used to regulate the output voltage of the buck converter of CPL (see Figure 2). Thus, once the output voltage and resistive load are constant, the output power ($P_L = v_{C1}^2/R_L$) will be constant. For a lossless converter $P_{CPL} = v_{C2}i_{o2} = P_L$, that exhibits a positive instantaneous impedance ($v_{C2}/i_{o2} > 0$), when input voltage decreases, input current increases and vice versa. This exhibits a negative incremental impedance ($\Delta v_{C2}/\Delta i_{o2} < 0$) which can have a negative effect on the stability of the system. Here, a comprehensive small-signal model of the shown CPL is

derived. For the buck converter between the main dc bus and resistive local bus if the switch turns on, it yields

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = v_{C2} - v_{C1} \\ C_1 \frac{dv_{C1}}{dt} = i_{L1} - i_{o1} \end{cases} \quad (1)$$

where i_{L1} , v_{C1} and i_{o1} are the inductor current, the capacitor voltage, the output current, respectively. Input current from main dc bus is $i_{o2} = i_{L1}$. If the switch turns off, it yields

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = -v_{C1} \\ C_1 \frac{dv_{C1}}{dt} = i_{L1} - i_{o1} \end{cases} \quad (2)$$

In this state, the input current from main dc bus is $i_{o2} = 0$. By using state-space averaging, the state-space function is derived as

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = -v_{C1} + d_1 v_{C2} \\ C_1 \frac{dv_{C1}}{dt} = i_{L1} - i_{o1} \end{cases} \quad (3)$$

and $i_{o2} = d_1 i_{L1}$, where d_1 is the duty cycle for on-state of the switch. Based on the results given in (3), the small-signal model of buck converter loaded with a resistive load R_L can be obtained as

$$\begin{cases} L_1 \frac{d\hat{i}_{L1}}{dt} = V_{C2} \hat{d}_1 + D_1 \hat{v}_{C2} - \hat{v}_{C1} \\ C_1 \frac{d\hat{v}_{C1}}{dt} = \hat{i}_{L1} - \frac{\hat{v}_{C2}}{R_L} \end{cases} \quad (4a)$$

$$\hat{i}_{o2} = D_1 \hat{i}_{L1} + \frac{V_{C1}}{R_L} \hat{d}_1 \quad (4b)$$

where the variables showing in capital letter represent the steady-state values and the variables with “ $\hat{\cdot}$ ” indicate the small-signal deviation. By considering the control diagram in Figure 2, the small signal model in frequency domain is achieved

$$\hat{d}_1(s) = (\hat{v}_{C1}^* - \hat{v}_{C1}) G_{pi1} \quad (5)$$

The closed-loop transfer function between the input voltage and input current is as follows:

$$Z_{in-CL}(s) = \left. \frac{\hat{v}_{C2}}{\hat{i}_{o2}} \right|_{\hat{v}_{C1}^*(s)=0} = \frac{R_L C_1 L_1 s^3 + L_1 s^2 + R_L (1 + V_{C2} K_{p1}) s + R_L V_{C2} K_{i1}}{R_L C_1 D_1^2 s^2 + (D_1^2 - K_{p1} D_1^2 V_{C2}) s - K_{i1} D_1^2 V_{C2}} \quad (6)$$

Closed-loop input impedance in (6) is more accurate compared to the traditional approximation by using pure negative resistance. The steady-state error for a step input can be calculated with the final value theorem and corresponds to the dc gain:

$$Z_{IN-CL} = -\frac{R_L}{D_1^2} = -\frac{V_{C2}^2}{P_{CPL}} \quad (7)$$

This behaves like a negative resistance. It means the loop gain and bandwidth of the feedback should be very high.

2.2. Small-signal model of the boost converter. The aforementioned discussion is for modeling of the buck converter used for the load-side converter. For the boost converter used in the source-side, the analysis is similar. In order to avoid repetition, no detailed procedure is shown below. By using the similar procedure in Section 2.1, one can obtain the final small-signal model of the boost converter as

$$\begin{cases} L_2 \frac{d\hat{i}_{L2}}{dt} = \hat{v}_g - (1 - D_2) \hat{v}_{C2} + V_{C2} \hat{d}_2 \\ C_2 \frac{d\hat{v}_{C2}}{dt} = (1 - D_2) \hat{i}_{L2} - I_{L2} \hat{d}_2 - \hat{i}_{o2} \end{cases} \quad (8)$$

where i_{L2} , v_{C2} , i_{o2} and d_2 follow the similar expressions compared to i_{L1} , v_{C1} , i_{o1} and d_1 ; only the index should be changed. The small-signal voltage-current characteristics of the CPL, according to (6), is given by

$$\hat{i}_{o2} = Z_{in-CL} \hat{v}_{C2} \quad (9)$$

However, in order to simplify the theoretical analysis, an ideal CPL (see (7)) is used which is $Z_{in-CL} = Z_{IN-CL}$. By transferring the linear small-signal model in (8) and (9) into frequency domain and combining the results, the control input-to-output voltage and control input-to-inductor current transfer functions are obtained as

$$G_{id}(s) = \frac{\hat{i}_{L2}(s)}{\hat{d}_2(s)} = \frac{C_2 V_{C2} s}{L_2 C_2 s^2 - \left(\frac{P_{CPL}}{V_{C2}^2} \right) L_2 s + (1 - D_2)^2} \quad (10)$$

$$G_{vd}(s) = \frac{\hat{v}_{C2}(s)}{\hat{d}_2(s)} = \frac{V_{C2} (1 - D_2) - I_{L2} L_2 s}{L_2 C_2 s^2 - \left(\frac{P_{CPL}}{V_{C2}^2} \right) L_2 s + (1 - D_2)^2} \quad (11)$$

The open-loop transfer functions in (10) and (11) have poles in the right half-plane (RHP). Therefore, the boost converter, when it is loaded with a CPL, is unstable. Due to the presence of right half-plane zero in (11), the boost converter is a non-minimum phase system. As a result, when the input signal increases, the system output shows a small undershoot before rising again and a high feedback system will exhibit instability. To cope with these issues an active damping control method is proposed in the next section.

3. Proposed Active Damping Method.

3.1. Stabilization of boost converters with CPLs. In this section, an active damping method based on inductor current feedback loop using PI control is presented to stabilize the system, as shown in Figure 2(b). Current mode control provides an inherent active damping for boost converters with CPLs and CPL is effectively transformed into a resistive load [29]. Furthermore, a voltage feedback loop regulates the converter's output voltage. In order to verify the effectiveness of the proposed method, first current control loop is neglected. Based on the control diagram shown in Figure 2(b), the small-signal model without current control loop and inertia response loop is achieved

$$\hat{d}_2(s) = (\hat{v}_{C2}^* - \hat{v}_{C2}) G_{pi2} \quad (12)$$

By substituting (12) into (11), the closed-loop transfer function yields

$$\frac{\hat{v}_{C2}(s)}{\hat{v}_{C2}^*(s)} = \frac{(K_{p2}s + K_{i2})(V_g - I_{L2}L_2s)}{a_3s^3 + a_2s^2 + a_1s^1 + a_0} \quad (13)$$

where

$$\begin{aligned} a_3 &= L_2 C_2, \quad a_2 = - \left(K_{p2} I_{L2} L_2 + \frac{P_{CPL}}{V_{C2}^2} L_2 \right) \\ a_1 &= (1 - D_2)^2 + K_{p2} V_g - I_{L2} L_2 K_{i2}, \quad a_0 = K_{i2} V_g \end{aligned} \quad (14)$$

According to the Hurwitz stability criterion, transfer function (13) has a pair of RHP poles due to $a_2 < 0$. Therefore, in such a case, the system is not stable. In order to overcome this problem, a current control loop is implemented. The closed-loop transfer function by considering this loop is derived. Based on the control diagram shown in Figure 2(b), the small-signal model is obtained:

$$\hat{d}_2(s) = \left(\hat{i}_{L2}^* - \hat{i}_{L2} \right) G_{pi3} \quad (15)$$

By substituting (15) into (10), the closed-loop transfer function yields

$$\frac{\hat{i}_{L2}(s)}{\hat{i}_{L2}^*(s)} = \frac{(K_{p3}s + K_{i3}) C_2 V_{C2}}{a_2 s^2 + a_1 s + a_0} \quad (16)$$

where

$$a_2 = L_2 C_2, \quad a_1 = \left(K_{p3} C_2 V_{C2} - \frac{P_{CPL}}{V_{C2}^2} L_2 \right), \quad a_0 = (1 - D_2)^2 + K_{i3} C_2 V_{C2} \quad (17)$$

In order to have a stable operating point, a necessary condition is

$$K_{p3} C_2 V_{C2} > \frac{P_{CPL}}{V_{C2}^2} L_2 \quad (18)$$

For a specific range of K_{p3} , condition (18) is satisfied and therefore the system stability margin can be enhanced. The closed-loop transfer function between output voltage with respect to the control input yields

$$\frac{\hat{v}_{C2}(s)}{\hat{v}_{C2}^*(s)} = \frac{(V_g - I_{L2} L_2 s) (K_{p2} s + K_{i2}) (K_{p3} s + K_{i3})}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s^1 + a_0} \quad (19)$$

where

$$\begin{aligned} a_4 &= L_2 C_2 \\ a_3 &= K_{p3} C_2 V_{C2} - L_2 P_{CPL} / V_{C2}^2 - K_{p2} K_{p3} L_2 I_{L2} \\ a_2 &= (1 - D_2)^2 + K_{i3} C_2 V_{C2} + K_{p2} K_{p3} V_g - (K_{i2} K_{p3} + K_{p2} K_{i3}) L_2 I_{L2} \\ a_1 &= (K_{i2} K_{p3} + K_{p2} K_{i3}) V_g - K_{i2} K_{i3} L_2 I_{L2} \\ a_0 &= K_{i2} K_{i3} V_g \end{aligned} \quad (20)$$

By selection of proper control parameters, the system stability margin can be enhanced. As shown in Figure 3, when the inductor current feedback is not activated (Equation (13)) and more accurate dynamic model of CPL (Equation (6)) is used, instable poles can be found in z domain that are $0.97 \pm j 0.48$. When the inductor current feedback is activated (Equation (19)), the unstable poles are forced to migrate into the unit circle. Hence, the system stability is guaranteed. In particular, the above poles are moved to $0.6 \pm j 0.08$.

3.2. Inertia response improvement of boost converters with CPLs. As already mentioned, the most important issue in dc MGs that affects dynamic performance and stability is the low inertia and damping property. In dc MGs, the energy stored in the dc

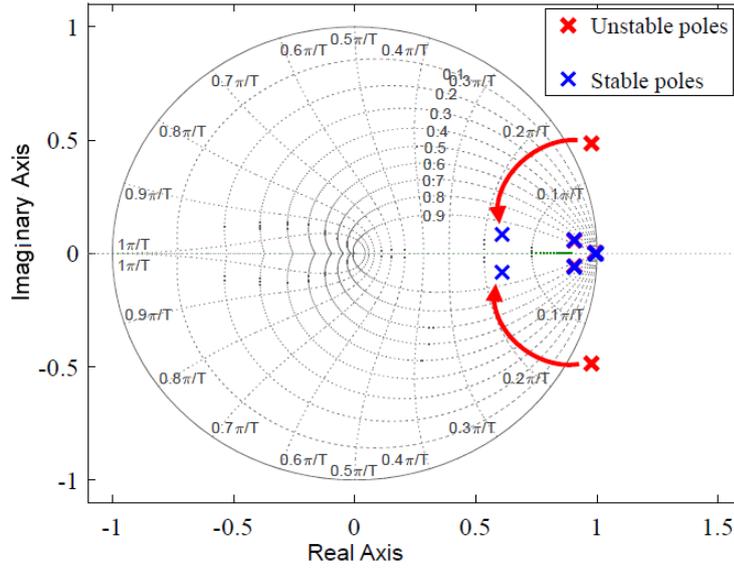


FIGURE 3. The poles of closed-loop system with and without current loop

capacitors creates a kind of inertia response for dc voltage. To clarify the effectiveness of this idea, the small-signal equation of (8) can be described as

$$\frac{d\hat{v}_{C2}}{dt} = \frac{1}{C_2} \left[(1 - D_2) \hat{i}_{L2} - I_{L2} \hat{d}_2 - \hat{i}_{o2} \right] \quad (21)$$

According to (21), the larger C_2 decreases the rate of change of voltage (RoCoV) and counteracts rapid change of the dc bus voltage. Since the dc capacitance is smaller than the rotational inertia of conventional ac grids and damping is not sufficiently large, the dc MG suffers from poorly damped dynamics. A solution toward increasing inertia and damping of these systems is to provide additional capacitance and damper virtually. The virtual inertia control mimics the behavior of SMs using an advanced control of the converter and energy storage system, enhancing system inertia and damping properties. The well-known SM small-signal swing equation can be represented in terms of power as [17]

$$J\omega_n \frac{d\hat{\omega}}{dt} + D_p \hat{\omega} = \hat{P}_{in} - \hat{P}_{out} \quad (22)$$

where J , D_p , ω , ω_n , P_{in} and P_{out} are the moment of inertia, the damping power coefficient, the rotor angular frequency, the nominal angular frequency, input mechanical power and output electrical power, respectively. Inspired by (22), a virtual inertia control strategy is implemented in inductor current loop as follows

$$\hat{i}_{L2}^* = -C_v \frac{d\hat{v}_{C2}}{dt} - D_v \hat{v}_{C2} \quad (23)$$

where C_v and D_v are the virtual capacitance and virtual damping, respectively. Since the proposed control is at the inner current control loop, it has to be faster than the outer voltage level control and provides a fast inertia response during load variations. Meanwhile, the bandwidth of the inner current loop of the boost converter (G_{pi3}) is high enough to track the inductor current reference variation. Substituting (23) and (15) into (21) yields

$$(C_2 + C'_v) \frac{d\hat{v}_{C2}}{dt} + D'_v \hat{v}_{C2} = -\hat{i}_{o2} \quad (24)$$

where $C'_v = (1 - D)C_v$ and $D'_v = (1 - D)D_v$. It can be seen from (24) that the virtual capacitance and damping coefficient are increased during load changes. As a result, the inertia and damping of the dc MG are improved. Figure 2(b) shows the proposed inertia response control loop that is applied in inner current control loop. The pure differentiator of the virtual capacitance in the proposed inertia response strategy may bring undesired high frequency noises to the system. This problem can be solved by constructing a first-order low-pass filter (LPF) in series with the virtual capacitance feedback. By considering LPF and applying Laplace transform, (23) can be rewritten as

$$i_{L2}^*(s) - I_{L2}^* = -(C_v s G_{LPF} + D_v) \hat{v}_{C2}(s) \tag{25}$$

where, $G_{LPF} = 1/(\tau s + 1)$ and τ is the time constant of the LPF. According to (8), (9), and Figure 2(b), the small-signal closed-loop transfer function between $v_{C2}(s)$ and $v_{C2}^*(s)$ is obtained as follows

$$G_T(s) = \frac{\hat{v}_{C2}}{\hat{v}_{C2}^*} = \frac{G_{vd} G_{pi2} G_{pi3}}{1 + G_{pi3} G_{id} + G_{pi3} G_{vd} (G_{pi2} + C_v s G_{LPF} + D_v)} \tag{26}$$

Figure 4 shows the step responses of $G_T(s)$ in (26) for 20% change in voltage reference. Figures 4(a) and 4(b) show dc bus voltage change for various values of C_v and D_v when one is fixed to zero. From Figure 4(a), the dc bus voltage would smoothly change and the RoCoV is lower when C_v increases. This means that the inertia of the dc MG is larger. Thereby, the value of C_v denotes the synthetic inertia of the dc MG. However, by increasing C_v the system damping decreases and is prone to cause the dc bus voltage oscillation. This problem can be solved by increasing damping coefficient (D_v) that effectively eliminates the low-frequency voltage oscillations, as shown in Figure 4(b). A trade-off may be considered between the voltage deviation and settling time for selecting the inertia and damping coefficients.

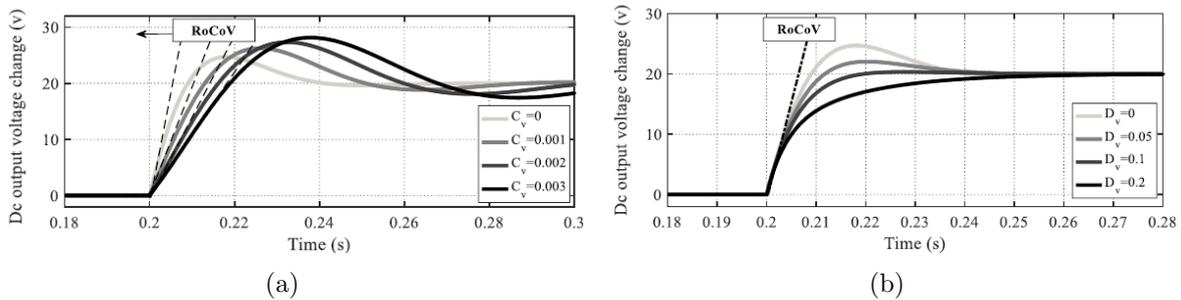


FIGURE 4. Step responses of $G_T(s)$: (a) various values of C_v , $D_v = 0.1$, $P_{CPL} = 1$ kW, and $\tau = 0.2$ ms, (b) various values of D_v , $C_v = 0.001$, $P_{CPL} = 1$ kW, and $\tau = 0.2$ ms

The effectiveness of the proposed inertia response is verified under input voltage change and load variation. Figures 5 and 6 show the dc bus voltage change for 10% step-change in input voltage and 10% step-change in load power, respectively. In both Figure 5 and Figure 6 (similar to Figure 4) when C_v and/or D_v increase (decrease), the rate of voltage deviation and voltage deviation is decreased (increased), respectively. Meanwhile, the parameters of inertia response have no influence on the steady-state performance. The proposed control parameters will have to ensure small-signal stability due to small disturbances or load perturbations at steady-state operation.

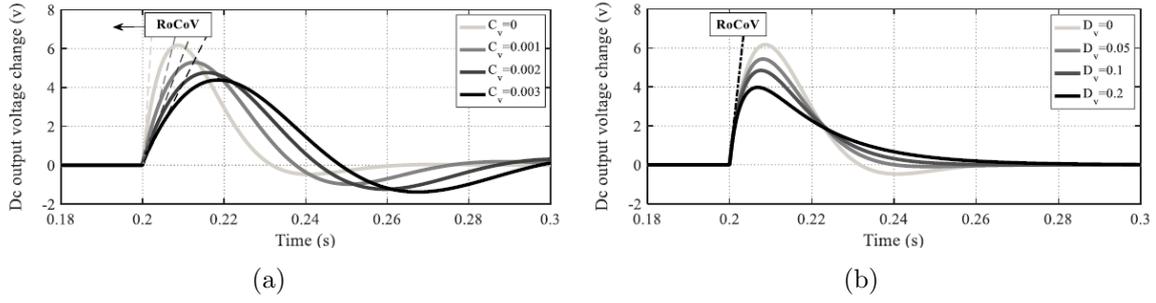


FIGURE 5. Step-change in input voltage: (a) various values of C_v , $D_v = 0.1$, $P_{CPL} = 1$ kW, and $\tau = 0.2$ ms, (b) various values of D_v , $C_v = 0.001$, $P_{CPL} = 1$ kW, and $\tau = 0.2$ ms

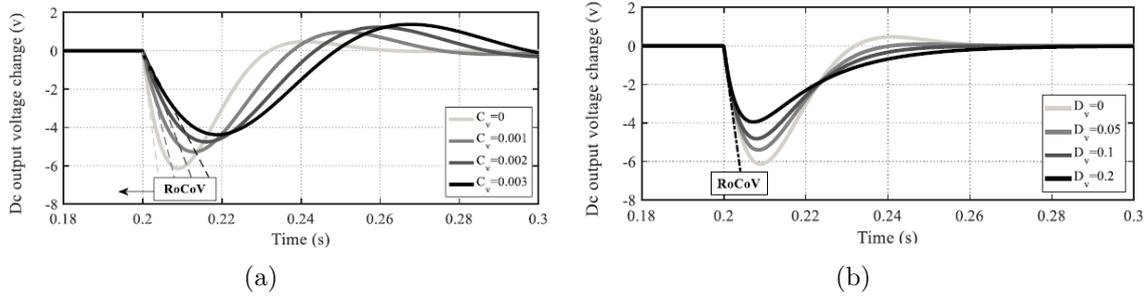


FIGURE 6. Step-change in load power: (a) various values of C_v , $D_v = 0.1$, and $\tau = 0.2$ ms, (b) various values of D_v , $C_v = 0.001$, and $\tau = 0.2$ ms

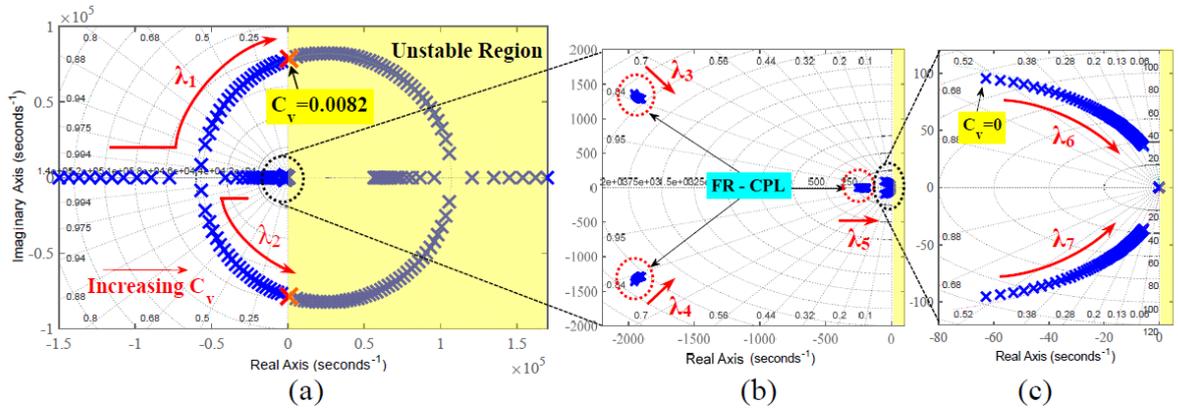


FIGURE 7. Trace of the system eigenvalues for: (a) varying C_v while $D_v = 0.1$, $P_{CPL} = 1$ kW, and $\tau = 0.2$ ms, (b) a zoomed view of (a) in origin, (c) a zoomed view of (b)

4. Stability Analysis and Parameter Selection. In this section, small-signal stability of the boost converter loaded by dynamic CPL (Equation(6)), is studied via analysis of the system eigenvalues using the transfer function derived in (26). Therefore, for the proposed control strategy, there are three parameters to be considered, namely, the virtual capacitance (C_v), damping coefficient (D_v), and the low-pass filter time constant (τ). In Figure 7, the eigenvalues of the entire system are plotted when C_v increases. The group of poles have low sensitive to C_v variety (see Figure 7(b)). The groups labeled fast-response

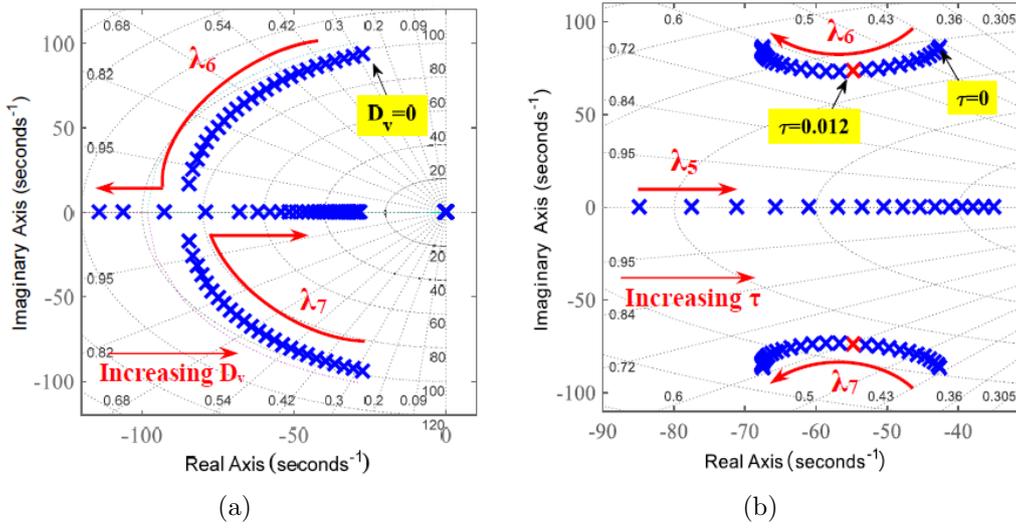


FIGURE 8. Trace of the dominant poles for: (a) varying D_v while $C_v = 0.001$, $P_{CPL} = 1$ kW, and $\tau = 0.2$ ms, (b) varying τ while $C_v = 0.001$, $D_v = 0.1$, and $P_{CPL} = 1$ kW

CPL (FR-CPL) are associated with the dynamic CPL represented in (6). It can be seen from Figure 7(a) that with increasing C_v , the two poles λ_1 and λ_2 move towards unstable region and finally becomes unstable when it exceeds 0.0082. These poles are far away from the origin point so their impact on the control system can be neglected. The dominant poles are closely related to eigenvalues λ_6 and λ_7 , as shown in Figure 7(c). By increasing C_v , damping ratio and the natural frequency of the complex conjugate eigenvalues (λ_6 and λ_7) continual decrease, so the system is more prone to low-frequency oscillation (see Figure 4(a)). Figure 8(a) shows the trajectory of dominant poles when D_v increases from 0 to 0.5. By increasing D_v , the damping ratio of dominant poles increases and the response speed is decreased as shown in Figure 4(b). Figure 8(b) shows the dominant low-frequency modes of the system when the time constant of the LPF increases from 0 to 30 ms. By increasing τ , the damping factor of the system is improved. As it is observed, there is also an inflection point for the low-pass filter time constant in the system root-locus diagram. Therefore, the inflection point of system root-locus will be the optimal one for the time constant, namely, $\tau = 12$ ms. Accordingly, the stability margin of the system is improved.

5. Simulation Results. In order to validate the effectiveness of the proposed control method, the test system of Figure 2, is simulated in MATLAB/Simulink. The system parameters are given in Table 1.

5.1. Case I: activation and deactivation of the active damping. Performance of the active damping method based on inductor current feedback is shown in the waveform of dc bus voltage depicted in Figure 9. Before $t = 0.2$ s, the active damping is not activated. It can be seen that a divergent oscillation occurs in the dc bus voltage profile and the system is unstable. At $t = 0.2$ s, the stabilizer is activated, and the dc bus voltage after a short dynamic process converges to the nominal voltage ($V_{C2} = 100$ V). Hence, the system becomes stable. At $t = 0.5$ s, the inductor current feedback is deactivated. Due to the effect of CPL, the system becomes unstable.

5.2. Case II: applying the proposed virtual inertia response. The effectiveness of the proposed virtual inertia response is investigated in three scenarios i.e., step voltage

TABLE 1. System parameters of the dc MG

System	Parameters	Values	Parameters	Values
Source-side boost converter	L_2	0.1 mH	V_g	50 V
	C_2	0.8 mF	V_{C2}^*	100 V
	K_{i2}	30	K_{i3}	100
	K_{p2}	0.15	K_{p3}	0.02
Load-side buck converter	L_1	10 mH	V_{C2}	100 V
	C_1	0.1 mF	V_{C1}^*	50 V
	K_{i1}	10	K_{p1}	0.05
Load	R_L	2.5 Ω	P_{CPL}	1 kW

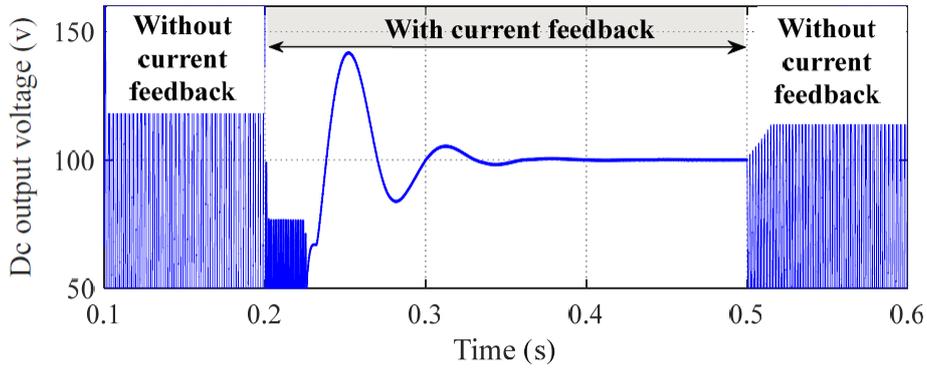


FIGURE 9. Activation and deactivation of the proposed controller

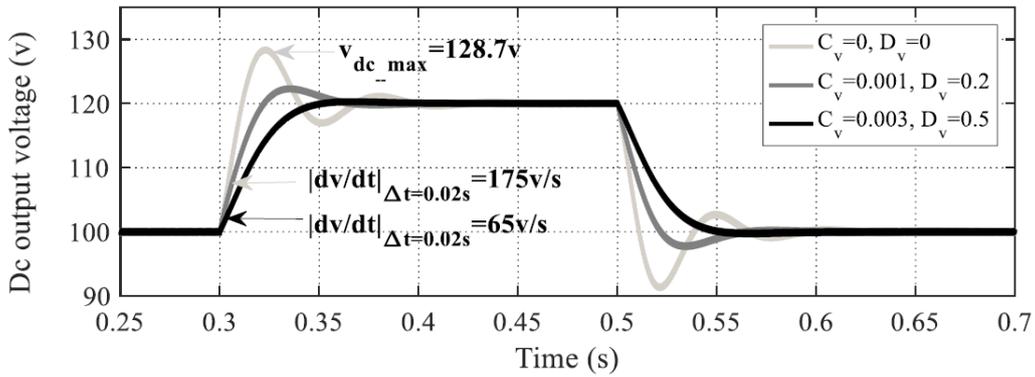


FIGURE 10. Dc output voltage under step change of voltage reference with and without the proposed virtual inertia loop

reference change ($\Delta V_{C2}^* = 0.2$ pu), step load power change ($\Delta P_{CPL} = 0.2$ pu), and step input voltage change ($\Delta V_g = 0.2$ pu), with $\tau = 0.2$ ms and the parameter values reported in Table 1. These changes are applied at $t = 0.3$ s and the system returns to the initial condition at $t = 0.5$ s.

Scenario 1: A 20% step change of voltage reference is applied under normal dc MG condition in Table 1. Figure 10 shows the comparison between the situations without (light gray line) and with (dark gray and black lines) virtual inertia response. It is obvious that the virtual inertia controller can improve the dc bus voltage performance due to significantly reduction of the RoCoV, the overshoot and oscillations. Thus, the dc MG stability margin is improved. As the C_v increases, the dc bus voltage would smoothly change and the RoCoV decreases. This means that the inertia of the dc MG is

increased. The RoCoV without the virtual inertia loop is around 175 V/s. In contrast, when the proposed virtual inertia loop shown in Figure 2(b) is activated RoCoV can be limited to be 65 V/s. Therefore, a 63% RoCoV reduction is achieved with the proposed virtual inertia method. However, by increasing C_v the system damping decreases and is prone to cause the dc bus voltage oscillation. This problem can be solved by increasing damping coefficient (D_v) that effectively eliminates the low-frequency voltage oscillations. Hence, the maximum voltage deviation can be reduced from 8.7 V to 0, indicating a 100% improvement over the case without virtual inertia. Similar observations can be obtained after $t = 0.5$ s, where the system is subject to a 20% step-down voltage reference change. However, virtual inertia response is more effective but increases the settling time of the dc bus voltage. Consequently, a trade-off between voltage deviation and settling time is made for selecting the inertia and damping coefficients.

Scenario 2: Figure 11 shows the comparison between the situations without and with virtual inertia response for a 20% step change of load power. At the beginning, $P_{CPL} = 1$ kW; when $t = 0.3$ s, a load step occurs and $P_{CPL} = 1.2$ kW; when $t = 0.5$ s, the load is reduced back to $P_{CPL} = 1$ kW. It can be seen that similar to Figure 10, the virtual inertia controller can improve the dc bus voltage performance and the dc MG stability margin is improved. The RoCoV without the virtual inertia loop is around 200 V/s. In contrast, when the proposed virtual inertia loop is activated RoCoV can be limited to be 75 V/s. Therefore, a 62% RoCoV reduction is achieved with the proposed virtual inertia method.

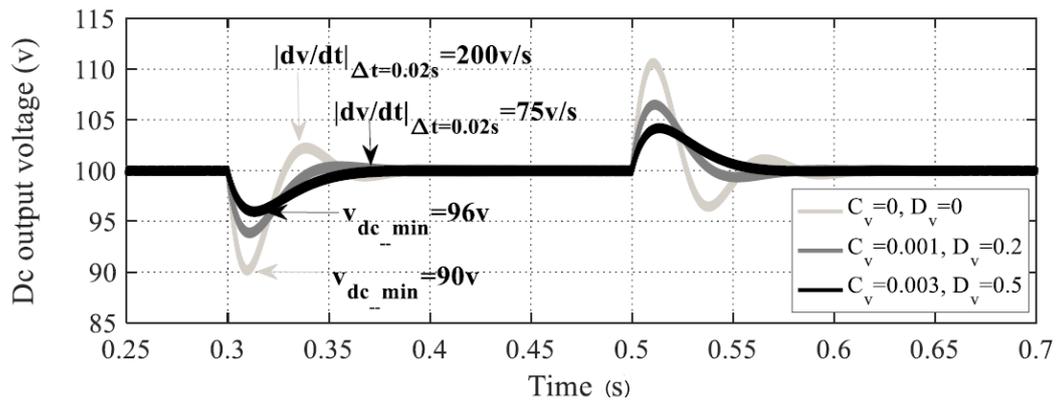


FIGURE 11. Dc output voltage under step change of load power with and without the proposed virtual inertia loop

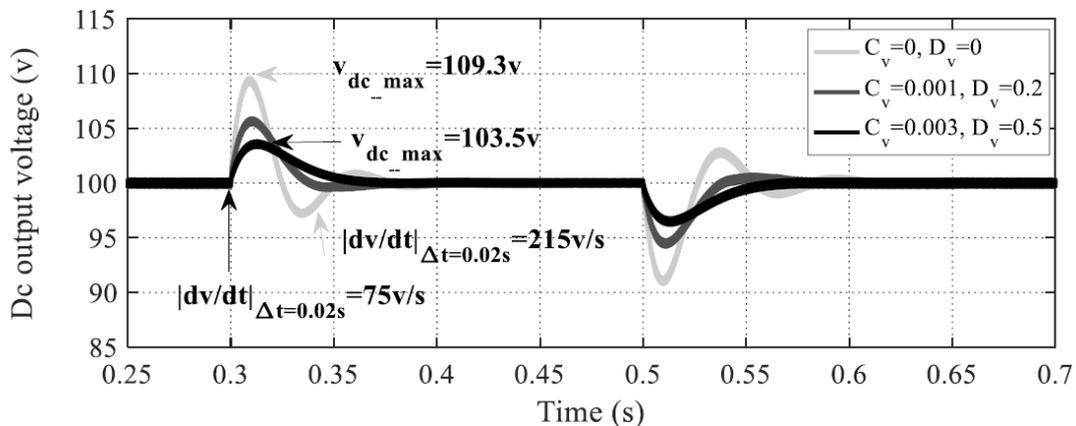


FIGURE 12. Dc output voltage under step change of input voltage with and without the proposed virtual inertia loop

Moreover, another critical parameter – the maximum voltage deviation can be reduced from 10 V to 4 V, indicating a 60% improvement over the case without virtual inertia. Similar scenario is studied in Figure 12 for 20% step change of input voltage.

6. Conclusions. To overcome the stability problems caused by CPLs and low inertia, this paper proposes an active damping control strategy to improve stability and inertia response of boost converters feeding CPL by implementing inductor current loop and inertia loop respectively. In the proposed method, the derivative feedback coefficient (C_v) in inertia loop mimics the virtual inertia. A low-pass filter is built in series with the proposed virtual capacitance for eliminating the high frequency oscillations brought by the pure differentiator. During variation in voltage reference, load power and power generation, the RoCoV is decreased when virtual capacitance increases. However, larger C_v causes bigger low-frequency oscillations and decreases damping; thereby, a proportional feedback gains (D_v) that mimics the damping factor is implemented to remove the oscillation. Comprehensive small-signal models of source-side boost converter and load-side buck converter are derived, and parameters selected are discussed based on root-locus analysis. The simulation results indicate that the virtual inertia control can provide inertia and damping properties.

It should be noted that, proposed method in this paper increases the settling time of the dc bus voltage and is not limited to the specific source of energy. This energy can be provided from different sources like battery, PV, and wind turbine. For instance, repeatedly sharp changes in output current will cause a significant increase of the operation temperature of Li-ion batteries, which would lower the system efficiency and shorten the lifetime of battery. Therefore, the use of a fast-dynamic auxiliary power source is necessary to feed the mentioned transient energy. Ultracapacitors can be the best choice for this purpose because in comparison with the batteries, they have higher specific power and also much longer lifetime. Future work should be focused on designing advanced fast and accurate ultracapacitor controllers.

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