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A MULTIPLIER WITH LOW JITTER USING MULTI-PHASE CLOCK DIVIDER

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Abstract. *In this paper, we propose the multiplier using the multi-phase clock divider design to realize the high-speed return from the system stand-by state in system operating state, and to reduce a time difference jitter of the output signal. The steady time difference jitter of the proposed multiplier becomes the 1 phase difference of the multi-phase clock by using the* $1 + 1/k$ *divider. It can also obtain the multiplication output signal from 2nd period of the input signal when the input signal is inputted in the system stop condition. These characteristics above of the proposed multiplier have been confirmed by using a Field Programmable Gate Array (FPGA) based on Verilog-HDL descriptions.*
Keywords: Multiplier, Multi-phase clock, Divider, Jitter

1. **Introduction.** Recently IC of the digital system has been remarkably improved, and many kinds of system clock generator are indispensable for this system. The power reduction of the interval is needed for lower power consumption of the whole system especially when it is used in the portable type information-processing equipment because the system stays in the stand-by state longer [1]. Therefore, the clock generation circuit should be stopped in the system while it is in the stand-by state. But it must quickly generate the clock, when it returns from the stand-by state [2].

The phase locked loop (PLL) is widely used as a clock generation circuit. However, since PLL needs some period of the input clock in the pull-in time before the output clock is stabilized [3], it is not possible to make a high-speed return from the system stop condition in the system operating state. Therefore, it is not possible to stop PLL in the system stand-by.

On the other hand, the clock generation circuit, which derives from the dividing technology, is easily made on circuit design, and can make a high-speed return from the system stand-by state in the system operating state. However, the circuit design had to be made over again according to conditions because the time difference jitter of the output signal generates 1 pulse width of the base clock which controls the circuit [4]. Also, in this multiplier, the output clock did not follow the input clock, when the reset signal was not input, and it could not obtain the multiplication output clock with the constant pulse interval.

In this paper, we propose the multiplier using the multi-phase clock divider design to realize the high-speed return from the system stand-by state in the system operating state and to reduce a time difference jitter of the output signal [5,6]. In the proposed